CURRENT CAPABILITY OF VSUP AND VAUX[2:0]

Product Family: **EM850X**

Part Number: EM8500

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ABSTRACT

The EM85XX offers a NVM containing all the configuration parameters. This document describes how to setup the registers linked to output drive capability of the supplies VSUP and VAUX[2:0] used without LDO in the NVM:

ABBREVIATIONS

NVM	Non-Volatile-Memory
MCU	Microcontroller Unit
STS	Short term storage element (capacitor connected to VDD_STS)
LTS	Long term storage element (rechargeable battery connected to VDD_LTS)
HRV	Harvester, main source of energy (solar or TEG)
VLD	Voltage Level Detector
Vref	Voltage level detector reference level
Vlvl	Voltage level detector LSB (71.88mV)
Vbat	Battery voltage connected to VDD_LTS
VSUP	Main output supply for application
VAUX[i]	2 independent auxiliary supplies for application
R_{BAT}	Battery internal resistivity
$R_{SW\_LTS\_STS}$	STS to LTS switch resistivity
R_{SW_VSUP}	STS to VSUP switch resistivity
R_{SW_VAUXi}	STS to VAUX*i* switch resistivity
I_{TOT}	Total current flowing from LTS to VSUP and/or VAUX*i*
I_{STD}	Total current flowing from LTS to VSUP and/or VAUX*i* in normal mode (low power)
I_{PEAK}	Total current flowing from LTS to VSUP and/or VAUX*i* in high mode

1. SCOPE

The EM8500 delivers 4 output supplies:

1. VSUP: main supply output usually used for MCU
2. VAUX[2:0]: 3 supply outputs used for peripherals such as RF, sensors, actuator etc…

   Each supply output can be directly connected to STS or regulated. When the LDO is used, the maximum current the EM8500 can deliver is limited by the LDO drive capability. This document describes the way to configure the device when VSUP and/or VAUX[2:0] are directly connected to STS.

The following registers are involved for that action:

Register name	Address	Description
reg_v_bat_min_hi_con	0x0A	Minimum battery and application voltage when STS and LTS are connected, form an hysteresis with **v_bat_min_lo**
reg_v_bat_min_lo	0x0B	Absolute minimum value of the battery and the application
reg_v_apl_max_hi	0x0C	Absolute maximum application voltage (ignored if set to 0xFF)
reg_v_apl_max_lo	0x0D	Maximum application voltage low level of hysteresis (ignored if set to 0xFE)
reg_ldo_cfg	0x0E	Configuration of the LDO
reg_vaux_cfg	0x10	Configuration of VAUX[2:0]

Table 1: List of Registers Related to Maximum Current Driven on VSUP and VAUX

The default value after reset or start-up of the registers listed in Table 1 is contained in a NVM memory at the following related addresses:

Register name	**Register Address**	**Related address in NVM**	
reg_v_bat_min_hi_con	0x0A	eeprom10	0x4A
reg_v_bat_min_lo	0x0B	eeprom11	0x4B
reg_v_apl_max_hi	0x0C	eeprom12	0x4C
reg_v_apl_max_lo	0x0D	eeprom13	0x4D
reg_ldo_cfg	0x0E	eeprom14	0x4E
reg_vaux_cfg	0x10	eeprom16	0x50

Table 2: Mapping of Registers in EEPROM

Note: the offset between the register addresses and related address in NVM is 0x40

2. DISABLE THE LDO

2.1 VSUP LDO

This part describes the way to configure the EM8500 product family, when no LDO is used. There are two conditions to keep the LDO on VSUP always disabled:

1. Set the register *reg_ldo_cfg.frc_ulp_ldo* = '0'
2. The voltage on STS shall be always < **v_apl_max_lo**

The easiest way to ensure that STS is always lower than v_apl_max_lo is to configure the device as follows:
reg_v_apl_max_hi = 0xFF
reg_v_apl_max_lo= 0xFE

2.2 VAUX LDO

To ensure the VAUX LDO is always disabled, the device shall be configured as follows:
reg_vaux_cfg = 0x00

3. CURRENT FLOW

The storage elements STS and LTS are considered as connected in that description. It is not recommended to drive high current on VSUP and VAUX when STS and LTS are disconnected.

The current flows from the battery to VSUP and VAUX as follows:

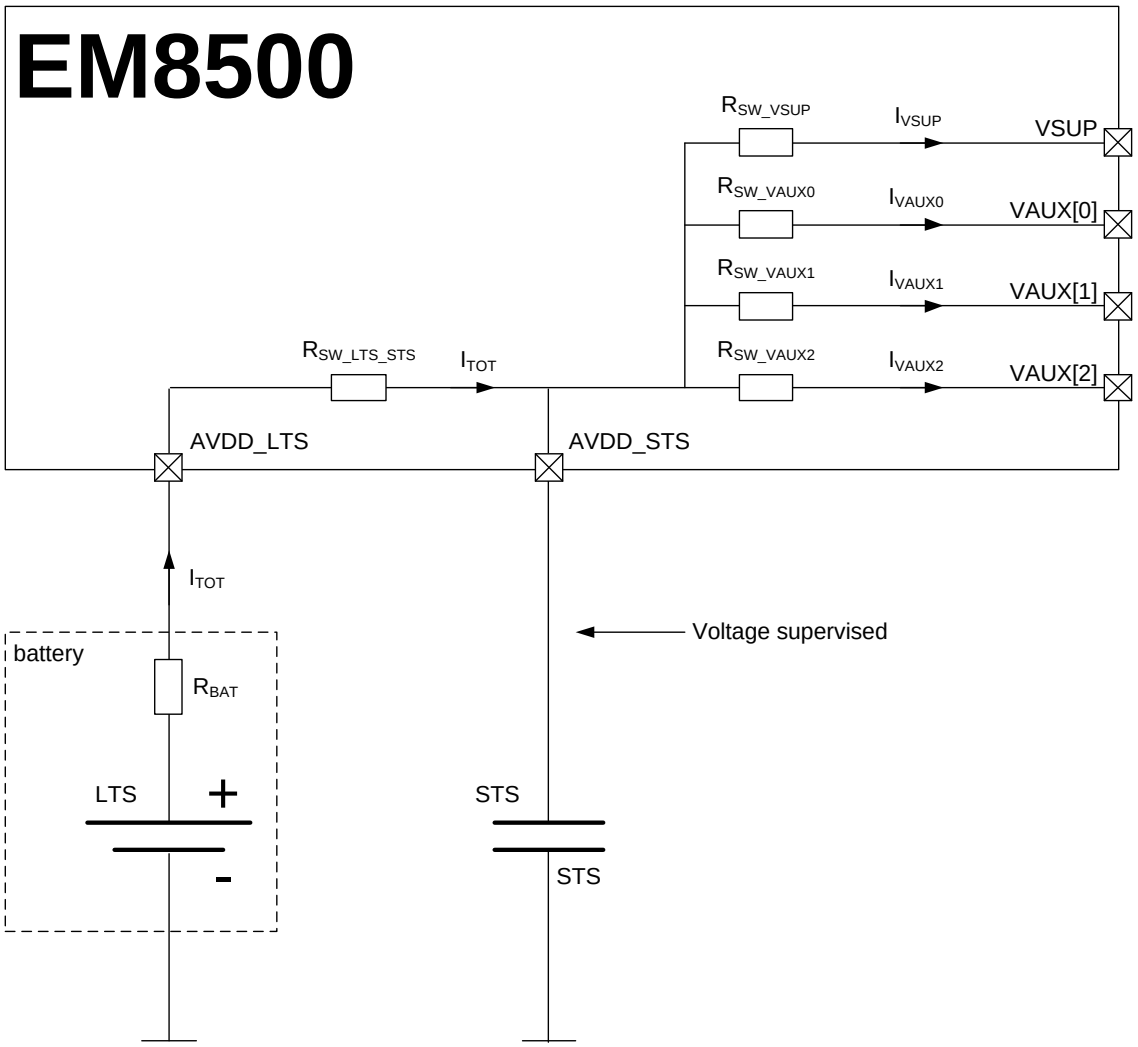

Figure 1: Current Flow Diagram

The current driven on VSUP and/or VAUX will generate a voltage drop on LTS and STS due to the different switches resistivity.

When STS and LTS are connected the EM8500 supervises STS.

When STS is detected lower than v_bat_min_lo, it disables VSUP and VAUX[2:0] to protect the system against overload.

4. REGISTER V_BAT_MIN_HI_CON CALCULATION

We consider 2 current levels:

1. Standard current I_{std}: total current load on VSUP and VAUX[2:0] in normal mode
2. Peak current I_{peak}: total peak current load on VSUP and VAUX[2:0] in high consumption mode

We consider the following worst case scenario:

The total charge current I_{TOT} is the sum of currents loaded on VSUP and VAUX[2:0].

The EM8500 is in normal mode and therefore I_{TOT} = I_{std}. The worst case is considered here – STS = v_bat_min_hi_con at the moment the current peak I_{peak} is driven on VSUP and/or VAUX[2:0]. The voltage on LTS and STS drops but shall remain above v_bat_min_lo to keep the system working.

The following timing diagram illustrates this scenario:

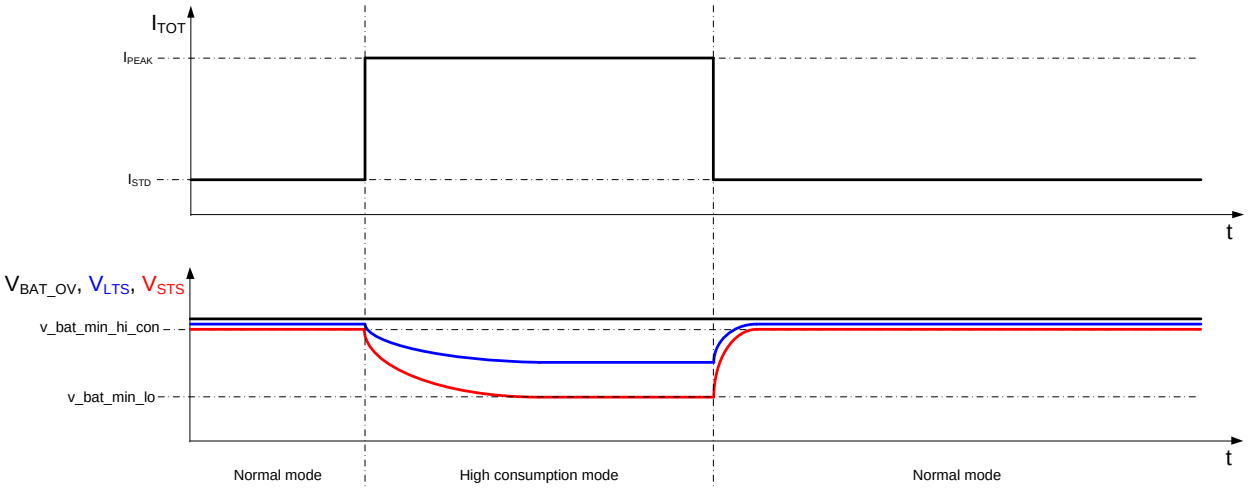

Figure 2: Worst Case Scenario Timing Diagram

The minimum delta between v_bat_min_hi_con and v_bat_min_lo shall follow the following rules:

$$reg\_v\_bat\_min\_hi\_con \geq \text{trunc}\left(\frac{(I_{PEAK}-I_{STD})\cdot(R_{BAT}+R_{SW\_LTS\_STS})}{min(V_{lvl})}\right)+reg\_v\_bat\_min\_lo+1$$

Equation 1: *reg_v_bat_min_hi_con* Calculation

Note: the values of $R_{SW\_LTS\_STS}$ and V_{lvl} are in the datasheet in table 4-3.
If the result of that equation is higher than the one calculated by the wizard, it shall replace it.

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