APPLICATION MANUAL

RV-8803-C7

DTCXO Temperature Compensated Real Time Clock / Calendar Module with I2C Interface

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RV-8803-C7

Highly accurate DTCXO Temperature Compensated Real Time Clock / Calendar Module with I²C Interface

1. OVERVIEW

- 32.768 kHz built-in “Tuning Fork” crystal oscillator
- Counters for hundredths, seconds, minutes, hours, date, month, year, century and weekday
- Factory calibrated temperature compensation
- Very high Time Accuracy
  - ± 1.5 ppm 0 to +50°C
  - ± 3.0 ppm -40 to +85°C
  - Aging compensation with OFFSET value
- I²C (up to 400 kHz) serial interface
- Periodic Countdown Timer Interrupt function
- Periodic Time Update Interrupt function (seconds, minutes)
- Alarm Interrupts for date, weekday, hour and minute settings
- External Event Input
- Programmable Clock Output for peripheral devices (32.768 kHz, 1.024 kHz, 1 Hz) with enable/disable function (CLKOE)
- Automatic leap year calculation (2000 to 2099)
- Wide operating voltage range: 1.5 V to 5.5 V
- Very low current consumption: 240 nA (V_{DD} = 3.0 V)
- Operating temperature range: -40 to +85°C
- Ultra-small and compact C7 package size, RoHS-compliant and 100% lead free: 3.2 x 1.5 x 0.8 mm
- Register compatible with Epson RX-8803SA/LC

1.1. GENERAL DESCRIPTION

The RV-8803-C7 is a highly accurate real-time clock/calendar module due to its built-in Thermometer and Digital Temperature Compensation circuitry (DTCXO). The Temperature Compensation circuitry is factory calibrated and results in highest time accuracy of ± 3.0 ppm across the temperature range from -40 to +85°C, and additionally offers an aging offset correction.
The RV-8803-C7 has the smallest package and the lowest current consumption among all temperature compensated RTC modules. Due to its special architecture the RV-8803-C7 provides a very low current consumption of 240 nA.

1.2. APPLICATIONS

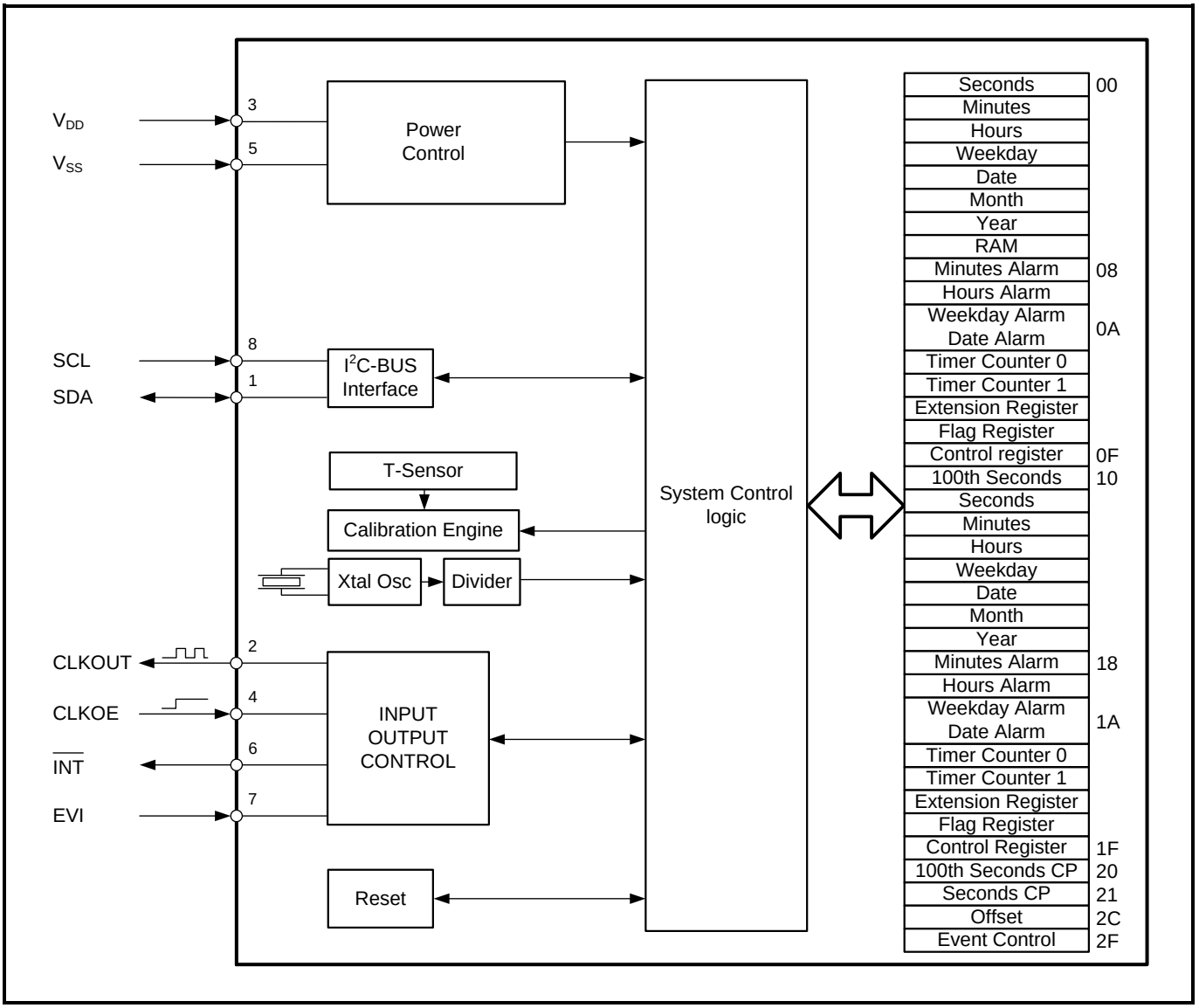
The RV-8803-C7 RTC module combines key functions with outstanding performance in an ultra-small ceramic package:

- Factory calibrated Temperature Compensation with temperature measuring every second
- Ultra-Low Power consumption
- Smallest RTC module (embedded XTAL) in an ultra-small 3.2 x 1.5 x 0.8 mm lead free ceramic package.

These unique features make this product perfectly suitable for many applications:

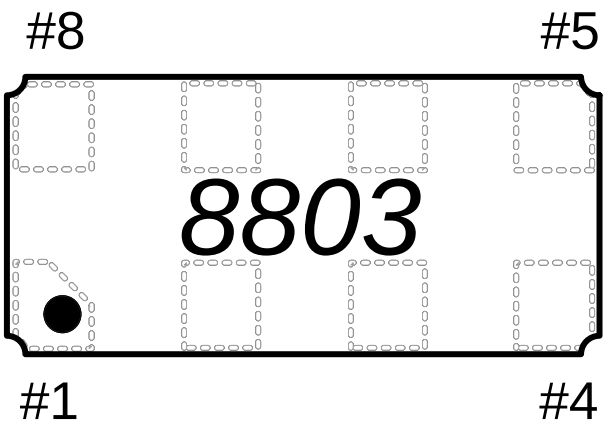
- Communication: IoT / Wireless Sensors and Tags / Handsets / Communications equipment
- Automotive: Navigation & Tracking Systems / Dashboard / Tachometers / Engine Controller / Car Audio & Entertainment Systems
- Metering: E-Meter / Heating Counter / Smart Meters / PV Converter
- Outdoor: ATM & POS systems / Surveillance & Safety systems / Ticketing Systems
- Medical: Glucose Meter / Health Monitoring Systems
- Safety: DSLR / Security & Camera Systems / Door Lock & Access Control
- Consumer: Gambling Machines / TV & Set Top Boxes / White Goods
- Automation: DSC / Data Logger / Home & Factory Automation / Industrial and Consumer Electronics

2. BLOCK DIAGRAM



2.1. PINOUT

C7 Package: (top view)



#1	SDA	#8	SCL
#2	CLKOUT	#7	EVI
#3	V_{DD}	#6	$\overline{INT}$
#4	CLKOE	#5	V_{SS}

2.2. PIN DESCRIPTION

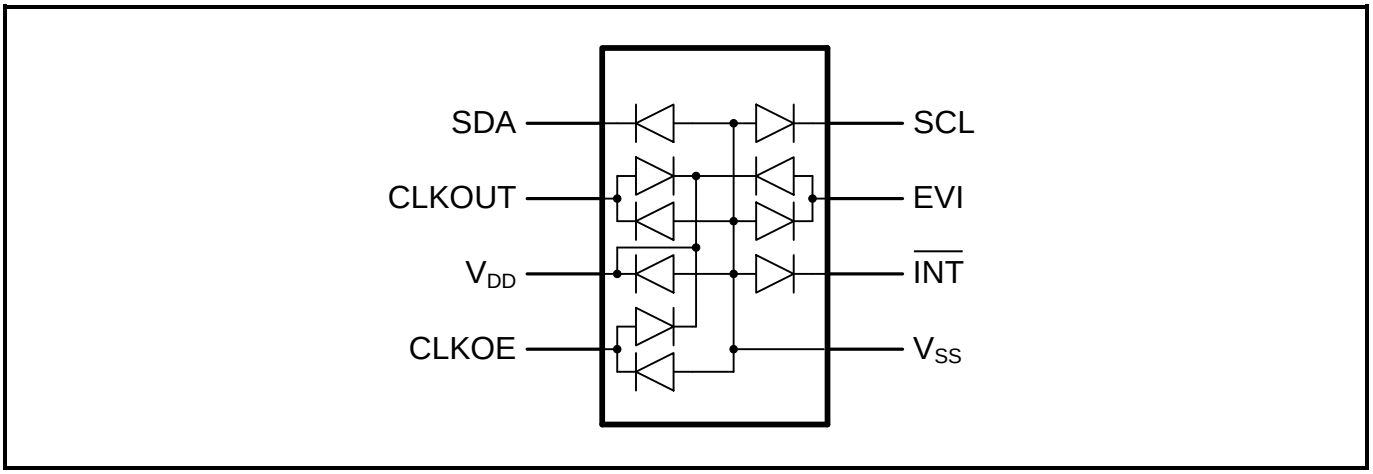
Symbol	Pin #	Description
SDA	1	I^2C Serial Data; open-drain; requires pull-up resistor.
CLKOUT	2	Clock Output; push-pull; controlled by CLKOE. If CLKOE is active HIGH, the CLKOUT pin drives the square wave of 32.768 kHz, 1.024 kHz or 1 Hz (Default value is 32.768 kHz). When CLKOE is tied to Ground, the CLKOUT pin is high impedance (tri-state).
V_{DD}	3	Power Supply Voltage.
CLKOE	4	Input to enable the CLKOUT pin. If CLKOE is active HIGH, the CLKOUT pin is in output mode. When CLKOE is tied to Ground, the CLKOUT pin is stopped and is high impedance (tri-state).
V_{SS}	5	Ground.
$\overline{INT}$	6	Interrupt Output; open-drain; requires pull-up resistor; Used to output Alarm, Periodic Countdown Timer, Periodic Time Update and External Event Interrupt signals.
EVI	7	External Event Interrupt Input.
SCL	8	I^2C Serial Clock Input; open-drain; requires pull-up resistor.

2.3. FUNCTIONAL DESCRIPTION

The RV-8803-C7 is a high accurate, ultra-low power CMOS based Real-Time-Clock Module with embedded 32.768 kHz Crystal. The Xtal 32.768 kHz clock itself is not temperature compensated.
The very high Time Accuracy and stability of ± 3.0 ppm over the full temperature range from -40°C to +85°C is achieved by the built-in Digital Temperature Compensation circuitry (DTCXO). The factory calibrated correction values are located in the EEPROM and are not accessible for the user. Additionally, there is an Offset Register customer use for aging correction.

The RV-8803-C7 provides standard Clock & Calendar function including seconds, minutes, hours (24), weekdays, date, months, years (with leap year calculation) and interrupt functions for an External Event, Periodic Countdown Timer, Periodic Time Update and Alarm. Beside the standard RTC functions, it includes an integrated Temperature Sensor, an External Event Input and 1 Byte of User RAM and offers an I^2C-bus (2-wire Interface). Further 2 Bytes can be used as User RAM when the Periodic Countdown Timer is not used (Timer Counter registers 0Bh, 1Bh and 0Ch, 1Ch) and further 3 Bytes when the Alarm function is not used (Alarm registers 08h, 18h; 09h, 19h and 0Ah, 1Ah).
The registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte.

2.4. DEVICE PROTECTION DIAGRAM



3. REGISTER ORGANIZATION

Registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte. The following tables Register Definitions (00h to 0Fh), (10h to 1Fh) and (20h to 2Fh) summarize the function of each register. In the table Register Definitions (00h to 0Fh) and (10h to 1Fh) the GPx bits (where x is between 0 and 5) are 6 register bits which may be used as general purpose storage. These bits are not described in the sections below. All of the GPx bits are cleared when the RV-8803-C7 powers up, and they can therefore be used to allow software to determine if a true Power-On-Reset has occurred or hold other initialization data.

- Address 00h to 0Fh: Basic time and calendar register — Adds RAM
- Address 10h to 1Fh: Extension register ① — Adds 100th Seconds counter
- Address 20h to 2Fh: Extension register ② — Capture buffer and Event control

Note: When writing or reading a specific function value into/from the Address range 00h to 0Fh the value will be automatically updated in the Address range 10h to 1Fh and vice versa.

In order to not corrupt the accuracy of the temperature compensation and the Time Capture function on the highest 100th Seconds resolution, it is not possible to freeze the clock and calendar register during read-out process, as it is common practice for other RTC's.
Since the time and calendar registers cannot be frozen, there might be a condition that the time registers are incremented while read-out. To avoid reading corrupted (partially incremented) data, special measures and procedures need to be applied (see TIME DATA READ-OUT).

3.1. REGISTER OVERVIEW

Register Definitions, Address 00h to 0Fh (Basic time and calendar register):

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Seconds	○	40	20	10	8	4	2	1
01h	Minutes	○	40	20	10	8	4	2	1
02h	Hours	○	○	20	10	8	4	2	1
03h	Weekday	○	6	5	4	3	2	1	0
04h	Date	○	○	20	10	8	4	2	1
05h	Month	○	○	○	10	8	4	2	1
06h	Year	80	40	20	10	8	4	2	1
07h	RAM	RAM data							
08h	Minutes Alarm	AE_M	40	20	10	8	4	2	1
09h	Hours Alarm	AE_H	GP0	20	10	8	4	2	1
0Ah	Weekday Alarm	AE_WD	6	5	4	3	2	1	0
	Date Alarm		GP1	20	10	8	4	2	1
0Bh	Timer Counter 0	128	64	32	16	8	4	2	1
0Ch	Timer Counter 1	GP5	GP4	GP3	GP2	2048	1024	512	256
0Dh	Extension Register	TEST	WADA	USEL	TE	FD		TD	
0Eh	Flag Register	○	○	UF	TF	AF	EVF	V2F	V1F
0Fh	Control Register	X		UIE	TIE	AIE	EIE	○	RESET
○ Read only. Always 0.									

Register Definitions, Address 10h to 1Fh (Extension register ①):

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	100th Seconds (Read Only)	80	40	20	10	8	4	2	1
11h	Seconds	○	40	20	10	8	4	2	1
12h	Minutes	○	40	20	10	8	4	2	1
13h	Hours	○	○	20	10	8	4	2	1
14h	Weekday	○	6	5	4	3	2	1	0
15h	Date	○	○	20	10	8	4	2	1
16h	Month	○	○	○	10	8	4	2	1
17h	Year	80	40	20	10	8	4	2	1
18h	Minutes Alarm	AE_M	40	20	10	8	4	2	1
19h	Hours Alarm	AE_H	GP0	20	10	8	4	2	1
1Ah	Weekday Alarm	AE_WD	6	5	4	3	2	1	0
	Date Alarm		GP1	20	10	8	4	2	1
1Bh	Timer Counter 0	128	64	32	16	8	4	2	1
1Ch	Timer Counter 1	GP5	GP4	GP3	GP2	2048	1024	512	256
1Dh	Extension Register	TEST	WADA	USEL	TE	FD		TD	
1Eh	Flag Register	○	○	UF	TF	AF	EVF	V2F	V1F
1Fh	Control Register	X		UIE	TIE	AIE	EIE	○	RESET

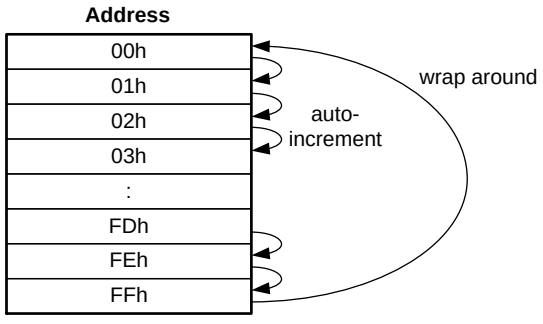
Register Definitions, Address 20h to 2Fh (Extension register ②):

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20h	100th Seconds CP (Read Only)	80	40	20	10	8	4	2	1
21h	Seconds CP (Read Only)	○	40	20	10	8	4	2	1
2Ch	Offset	○	○	OFFSET					
2Fh	Event Control	ECP	EHL	ET		○	○	○	ERST

3.1.1.AUTO-INCREMENTING

When address is automatically incremented, wrap around occurs from the address FFh to the address 00h (see figure below).

Auto-incrementing of the registers:



3.2. CLOCK REGISTERS

10h - 100th Seconds (Read Only)

This register holds the count of hundredths of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 99.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	100th Seconds (Read Only)	80	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	100th Seconds (Read Only)	00 to 99	Holds the count of hundredths of seconds, coded in BCD format. The 100th Seconds register is cleared to 00 when writing to the Seconds register or when setting the RESET bit to 1 or when the ERST bit is 1 in case of an External Event detection on EVI pin.

00h, 11h - Seconds

This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h, 11h(1)	Seconds	○	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	○	0	Read only. Always 0.
6:0	Seconds	00 to 59	Holds the count of seconds, coded in BCD format.

01h, 12h - Minutes

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h, 12h(1)	Minutes	○	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	○	0	Read only. Always 0.
6:0	Minutes	00 to 59	Holds the count of minutes, coded in BCD format.

02h, 13h - Hours

This register holds the count of hours, in two binary coded decimal (BCD) digits. Values will be from 00 to 23.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h, 13h(1)	Hours	○	○	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:6	○	0	Read only. Always 0.
5:0	Hours	00 to 23	Holds the count of hours, coded in BCD format.

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

3.3. CALENDAR REGISTERS

03h, 14h - Weekday

This register holds the current day of the week. Each bit represents one weekday that is assigned by the user. Values will range from 1 to 7. Do not set 1 to more than one bit.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h, 14h(1)	Weekday	○	7	6	5	4	3	2	1
	Reset	0	1	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	○	0	Read only. Always 0.
6:0	Weekday	1 to 7	Holds the weekday counter value. Do not set 1 to more than one bit.

Weekday	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Weekday 1	0	0	0	0	0	0	0	1
Weekday 2		0	0	0	0	0	1	0
Weekday 3		0	0	0	0	1	0	0
Weekday 4		0	0	0	1	0	0	0
Weekday 5		0	0	1	0	0	0	0
Weekday 6		0	1	0	0	0	0	0
Weekday 7 – Default value		1	0	0	0	0	0	0

04h, 15h – Date

This register holds the current day of the month, in two binary coded decimal (BCD) digits. Values will range from 00 to 31. The Reset value 00 after POR has to be replaced by a valid initial value (01 to 31). Leap years are correctly handled from 2000 to 2099.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h, 15h(1)	Date	○	○	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:6	○	0	Read only. Always 0.
5:0	Date	00 to 31	Holds the current date of the month, coded in BCD format. The Reset value 00 after POR has to be replaced by a valid initial value (01 to 31).

05h, 16h - Month

This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h, 16h(1)	Month	○	○	○	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	1

Bit	Symbol	Value	Description
7:5	○	0	Read only. Always 0.
4:0	Month	01 to 12	Holds the current month, coded in BCD format.

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

06h, 17h - Year

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h, 17h[1]	Year	80	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	Year	00 to 99	Holds the current year, coded in BCD format.

07h - RAM

This register holds the bits for general purpose use.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h	RAM	RAM data							
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	RAM	00h to FFh	User RAM

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

3.4. ALARM REGISTERS

08h, 18h – Minutes Alarm

This register holds the Minutes Alarm Enable bit AE_M and the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h, 18h(1)	Minutes Alarm	AE_M	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_M	Minutes Alarm Enable bit. Enables alarm together with AE_H and AE_WD (see USE OF THE ALARM INTERRUPT).	
		0	Minutes Alarm is enabled.
		1	Minutes Alarm is disabled.
6:0	Minutes Alarm	00 to 59	Holds the alarm value for minutes, coded in BCD format.

09h, 19h – Hours Alarm

This register holds the Hours Alarm Enable bit AE_H and the alarm value for hours, in two binary coded decimal (BCD) digits. Values will range from 00 to 23.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h, 19h(1)	Hours Alarm	AE_H	GP0	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_H	Hours Alarm Enable bit. Enables alarm together with AE_M and AE_WD (see USE OF THE ALARM INTERRUPT).	
		0	Hours Alarm is enabled.
		1	Hours Alarm is disabled.
6	GP0	0 or 1	Register bit for general purpose use.
5:0	Hours Alarm	00 to 23	Holds the alarm value for hours, coded in BCD format.

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

0Ah, 1Ah – Weekday/Date Alarm

This register holds the Weekday/Date Alarm Enable bit AE_WD. If the WADA bit is 0 (Bit 6 in Register 0Dh, 1Dh), it holds the alarm value for the day of the week (weekdays assigned by the user). Multiple days can be selected. Values will range from 0000001 to 1111111. If the WADA bit is 1, it holds the alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 2000 to 2099.

Weekday Alarm when WADA = 0 (Bit 6 in Register 0Dh, 1Dh)

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah, 1Ah(1)	Weekday Alarm	AE_WD	7	6	5	4	3	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_WD	Weekday/Date Alarm Enable bit. Enables alarm together with AE_M and AE_H (see USE OF THE ALARM INTERRUPT).	
		0	Weekday/Date Alarm is enabled.
		1	Weekday/Date Alarm is disabled.
6:0	Weekday Alarm	0000001 to 1111111	Holds the weekday alarm value. Multiple days can be selected.

Weekday Alarm	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Weekday 1 Alarm	0 or 1	0	0	0	0	0	0	1
Weekday 2 Alarm		0	0	0	0	0	1	0
Weekday 3 Alarm		0	0	0	0	1	0	0
Weekday 4 Alarm		0	0	0	1	0	0	0
Weekday 5 Alarm		0	0	1	0	0	0	0
Weekday 6 Alarm		0	1	0	0	0	0	0
Weekday 7 Alarm		1	0	0	0	0	0	0

Date Alarm when WADA = 1 (Bit 6 in Register 0Dh, 1Dh)

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah, 1Ah(1)	Date Alarm	AE_WD	GP1	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	AE_WD	Weekday/Date Alarm Enable bit. Enables alarm together with AE_M and AE_H (see USE OF THE ALARM INTERRUPT).	
		0	Weekday/Date Alarm is enabled
		1	Weekday/Date Alarm is disabled
6	GP1	0 or 1	Register bit for general purpose use.
5:0	Date Alarm	01 to 31	Holds the alarm value for the date, coded in BCD format.

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

3.5. PERIODIC COUNTDOWN TIMER CONTROL REGISTERS

0Bh, 1Bh – Timer Counter 0

This register is used to set the lower 8 bits of the preset value for the Periodic Countdown Timer.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh, 1Bh[1]	Timer Counter 0	128	64	32	16	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	Timer Counter 0	00h to FFh	The preset value for the Periodic Countdown Timer (lower 8 bit) (see USE OF THE PERIODIC COUNTDOWN TIMER).

0Ch, 1Ch – Timer Counter 1

This register is used to set the upper 4 bits of the preset value for the Periodic Countdown Timer.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch, 1Ch[1]	Timer Counter 1	GP5	GP4	GP3	GP2	2048	1024	512	256
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	GP2	0 or 1	Register bit for general purpose use.
6	GP3	0 or 1	Register bit for general purpose use.
5	GP4	0 or 1	Register bit for general purpose use.
4	GP5	0 or 1	Register bit for general purpose use.
3:0	Timer Counter 1	0h to Fh	The preset value for the Periodic Countdown Timer (upper 4 bit) (see USE OF THE PERIODIC COUNTDOWN TIMER).

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

3.6. EXTENSION REGISTER

0Dh, 1Dh – Extension Register

This register is used to specify the target for the Alarm Interrupt function and the Periodic Time Update Interrupt function and to select or set operations for the Periodic Countdown Timer.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh, 1Dh(1)	Extension Register	TEST	WADA	USEL	TE	FD		TD	
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	TEST	0	This is a manufacturer's test bit. Its value should always be 0. Avoid writing a 1 to this bit when writing in this register. Zero for normal operation.
6	WADA	Weekday Alarm / Date Alarm selection bit. This bit is used to specify either the Weekday or Date as the source for the Alarm Interrupt function.	
		0	Weekday is the source for the Alarm Interrupt function. – Default value
		1	Date is the source for the Alarm Interrupt function.
5	USEL	Update Interrupt Select bit. Specifies either Second or Minute update for the Periodic Time Update Interrupt function.	
		0	Second update (Auto reset time t_{RTN} = 500 ms). – Default value
		1	Minute update (Auto reset time t_{RTN} = 15.6 ms).
4	TE	Periodic Countdown Timer Enable bit. This bit controls the start/stop setting for the Periodic Countdown Timer Interruption function.	
		0	Stops the Periodic Countdown Timer Interrupt function. – Default value
		1	Starts the Periodic Countdown Timer Interrupt function (a countdown starts from a preset value).
3:2	FD	CLKOUT frequency selection. Sets the output frequency on the CLKOUT pin.	
		00	32.768 kHz – Default value
		01	1.024 kHz
		10	1 Hz
		11	32.768 kHz
1:0	TD	00 to 11	Timer source frequency selection. Sets the countdown source clock for the Periodic Countdown Timer Interrupt function. With this setting the Auto reset time t_{RTN} and the effect of the RESET bit is also defined. See table below (see also PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION).

TD Value	Timer source frequency	Countdown period	t_{RTN}	RESET bit
00	4.096 kHz – Default value	244.14 µs	122 µs	The RESET bit has no effect.
01	64 Hz	15.625 ms	7.183 ms	If the RESET bit = 1, the interrupt function is stopped.
10	1 Hz	1 s	7.183 ms	
11	1/60 Hz	60 s	7.183 ms	

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

3.7. FLAG REGISTER

0Eh, 1Eh – Flag Register

This register holds a variety of status bits. The register may be written at any time to clear any status flag.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh, 1Eh(1)	Flag Register	○	○	UF	TF	AF	EVF	V2F	V1F
	Reset	0	0	0	0	0	X	1	1

Bit	Symbol	Value	Description
7:6	○	0	Read only. Always 0.
5	UF	Periodic Time Update Flag (see PERIODIC TIME UPDATE INTERRUPT FUNCTION)	
		0	It can be cleared by writing a 0 to the bit.
		1	If set to 0 beforehand, indicates the occurrence of a Periodic Time Update Interrupt event.
4	TF	Periodic Countdown Timer Flag (see PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION)	
		0	It can be cleared by writing a 0 to the bit.
		1	If set to 0 beforehand, indicates the occurrence of a Periodic Countdown Timer Interrupt event.
3	AF	Alarm Flag (see ALARM INTERRUPT FUNCTION)	
		0	It can be cleared by writing a 0 to the bit.
		1	If set to 0 beforehand, indicates the occurrence of an Alarm Interrupt event.
2	EVF	External Event Flag (see EXTERNAL EVENT FUNCTION).	
		X	The Reset value X depends on the voltage on the EVI pin at POR and has to be cleared by writing a 0 to the bit. Because EHL = 0 at POR, the low level is regarded as an External Event Interrupt. If X =1, a LOW level was detected on EVI pin. If X =0, no LOW level was detected on EVI pin.
		0	It can be cleared by writing a 0 to the bit.
		1	If set to 0 beforehand, indicates the occurrence of an External Event.
1	V2F	Voltage Low Flag 2	
		0	Read: No data loss detected. Write: The V2F bit is cleared to prepare for a next low voltage detection.
		1	Read: Set if the voltage crosses V_{LOW2} voltage and the data in the device are no longer valid. All registers must be initialized. It can be cleared by writing a 0 to the bit. The flag is also automatically set to 1 at power on reset (POR) and has to be cleared by writing a 0 to the bit. Write: The V2F bit remains unchanged.
0	V1F	Voltage Low Flag 1	
		0	Read: Temperature compensation is effective. Write: The V1F bit is cleared to prepare for a next low voltage detection.
		1	Read: Set if the voltage crosses V_{LOW1} voltage and the temperature compensation is stopped. It can be cleared by writing a 0 to the bit. The flag is also automatically set to 1 at power on reset (POR) and has to be cleared by writing a 0 to the bit. Write: The V1F bit remains unchanged.

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

3.8. CONTROL REGISTER

0Fh, 1Fh – Control Register

This register is used to control the interrupt event output from the $\overline{INT}$ pin and the stop/start status of clock and calendar operations.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh, 1Fh(1)	Control Register	X		UIE	TIE	AIE	EIE	○	RESET
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:6	X	0	Unused, but has to be 0 to avoid extraneous leakage.
5	UIE		Periodic Time Update Interrupt Enable
		0	No interrupt signal is generated on $\overline{INT}$ pin when a Periodic Time Update event occurs or the signal is cancelled on $\overline{INT}$ pin.
		1	An interrupt signal is generated on $\overline{INT}$ pin when a Periodic Time Update event occurs. The low-level output signal is automatically cleared after t_{RTN} = 500 ms (Second update) or t_{RTN} = 15.6 ms (Minute update).
4	TIE		Periodic Countdown Timer Interrupt Enable
		0	No interrupt signal is generated on $\overline{INT}$ pin when a Periodic Countdown Timer event occurs or the signal is cancelled on $\overline{INT}$ pin.
		1	An interrupt signal is generated on $\overline{INT}$ pin when a Periodic Countdown Timer event occurs. The low-level output signal is automatically cleared after t_{RTN} = 122 µs (TD = 00) or t_{RTN} = 7.813 ms (TD = 01, 10, 11).
3	AIE		Alarm Interrupt Enable
		0	No interrupt signal is generated on $\overline{INT}$ pin when an Alarm event occurs or the signal is cancelled on $\overline{INT}$ pin.
		1	An interrupt signal is generated on $\overline{INT}$ pin when an Alarm event occurs. This setting is retained until the AF bit value is cleared to 0 (no automatic cancellation).
2	EIE		External Event Interrupt Enable
		0	No interrupt signal is generated on $\overline{INT}$ pin when an External Event on EVI pin occurs.
		1	An interrupt signal is generated on $\overline{INT}$ pin when an External Event on EVI pin occurs. This setting is retained until the EVF bit value is cleared to 0 (no automatic cancellation).
1	○	0	Read only. Always 0.
0	RESET	0	The reset is released.
		1	Values less than seconds of the counter in the clock and calendar circuitry are reset to 0 (2 Hz to 16 kHz), and the clock also stops. The 100th Seconds register is also reset to 0. The Periodic Countdown Timer, Periodic Time Update and Alarm Interrupts do not occur.

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

3.9. OFFSET REGISTER

2Ch – Offset Register

This register holds the OFFSET value for the aging correction.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2Ch	Offset	○	○	OFFSET					
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:6	○	0	Read only. Always 0.
5:0	OFFSET	-32 to +31	The amount of the effective frequency offset. This is a two's complement number with a range of -32 to +31 adjustment steps (maximum correction range is roughly +/-7.4 ppm). The correction value of one LSB corresponds to 1/(32768*128) = 0.2384 ppm (see AGING CORRECTION).

OFFSET	Unsigned value	Two's complement	Offset value in ppm(*)
011111	31	31	7.391
011110	30	30	7.153
:	:	:	:
000001	1	1	0.238
000000	0	0	0.000
111111	63	-1	-0.238
111110	62	-2	-0.477
:	:	:	:
100001	33	-31	-7.391
100000	32	-32	-7.629

(*) Calculated with 5 decimal places (1/(32768*128) = 0.23842 ppm)

3.10. CAPTURE BUFFER/EVENT CONTROL REGISTERS

20h – 100th Seconds CP (Read Only)

This register holds a captured (copied) value of the 100th Seconds register, in two binary coded decimal (BCD) digits. The values are from 00 to 99.

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20h	100th Seconds CP (Read Only)	80	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7:0	100th Seconds CP (Read Only)	00 to 99	Holds a captured value of the 100th Seconds register, coded in BCD format.

21h - Seconds CP (Read Only)

This register holds a captured (copied) value of the Seconds register, in two binary coded decimal (BCD) digits. The values are from 00 to 59.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
21h	Seconds CP (Read Only)	○	40	20	10	8	4	2	1
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	○	0	Read only. Always 0.
6:0	Seconds CP (Read Only)	00 to 59	Holds a captured value of the Seconds register, coded in BCD format.

2Fh – Event Control

This register controls the event detection on the EVI pin. Depending of the EHL bit a high or a low signal can be detected. Moreover a digital glitch filtering can be applied to the EVI signal by selecting a sampling period in the ET field.

Addresses	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2Fh	Event Control	ECP	EHL	ET		○	○	○	ERST
	Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Value	Description
7	ECP		Event Capture Enable
		0	Disables the Event Capture.
		1	An External Event detected on pin EVI will cause a capture of the Seconds and the 100th Seconds, i.e. they are copied into the Seconds CP and 100th Seconds CP registers.
6	EHL		Event High/Low detection Select
		0	The LOW level is regarded as the External Event Interrupt on pin EVI.
		1	The HIGH level is regarded as the External Event Interrupt on pin EVI.
5:4	ET		Event Filtering Time set. Applies a digital filtering to the EVI pin by sampling the EVI signal. Edge and level detection when ET = 01, 10 or 11 (see USE OF THE EXTERNAL EVENT).
		00	No filtering. Edge detection (minimal pulse time is 30.5 µs). – Default value
		01	3.9 ms sampling period (256 Hz).
		10	15.6 ms sampling period (64 Hz).
		11	125 ms sampling period (8 Hz).
3:1	○	0	Read only. Always 0.
0	ERST		Event Reset. This bit is used for a hardware-based time adjustment (synchronizing) (see USE OF THE EXTERNAL EVENT).
		0	No reset if an External Event is detected.
		1	In case of an External Event detection at the EVI pin, the counters at below the second are reset to 0 (2 Hz to 16 kHz). This means that the 100th Seconds Register (100 Hz) is reset to 0. Moreover, the 100th Seconds CP and Seconds CP registers are also reset to 0, whatever the ECP value is. After the event detection, the ERST bit is reset to 0. Be aware that the setting back of the counters at below the second influences also the operation of the other three interrupt functions: - Periodic Countdown Timer Interrupt function - Periodic Time Update Interrupt function - Alarm Interrupt function When 1, the reset function may be cancelled when the ERST bit is set back to 0 before an event occurs.

3.11. REGISTER RESET VALUES SUMMARY

Address	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10h	100th Seconds (Read Only)	0	0	0	0	0	0	0	0
00h, 11h(1)	Seconds	0	0	0	0	0	0	0	0
01h, 12h(1)	Minutes	0	0	0	0	0	0	0	0
02h, 13h(1)	Hours	0	0	0	0	0	0	0	0
03h, 14h(1)	Weekday	0	1	0	0	0	0	0	0
04h, 15h(1)	Date	0	0	0	0	0	0	0	0
05h, 16h(1)	Month	0	0	0	0	0	0	0	1
06h, 17h(1)	Year	0	0	0	0	0	0	0	0
07h	RAM	0	0	0	0	0	0	0	0
08h, 18h(1)	Minutes Alarm	0	0	0	0	0	0	0	0
09h, 19h(1)	Hours Alarm	0	0	0	0	0	0	0	0
0Ah, 1Ah(1)	Weekday Alarm / Date Alarm	0	0	0	0	0	0	0	0
0Bh, 1Bh(1)	Timer Counter 0	0	0	0	0	0	0	0	0
0Ch, 1Ch(1)	Timer Counter 1	0	0	0	0	0	0	0	0
0Dh, 1Dh(1)	Extension Register	0	0	0	0	0	0	0	0
0Eh, 1Eh(1)	Flag Register	0	0	0	0	0	X	1	1
0Fh, 1Fh(1)	Control Register	0	0	0	0	0	0	0	0
20h	100th Seconds CP (Read Only)	0	0	0	0	0	0	0	0
21h	Seconds CP (Read Only)	0	0	0	0	0	0	0	0
2Ch	Offset	0	0	0	0	0	0	0	0
2Fh	Event Control	0	0	0	0	0	0	0	0

(1) This specific function accessed in Address range 00h to 0Fh is automatically updated in Address range 10h to 1Fh and vice versa.

4. DETAILED FUNCTIONAL DESCRIPTION

4.1. POWER ON RESET (POR)

The power on reset (POR) is generated at start-up (see POWER ON AC ELECTRICAL CHARACTERISTICS). All registers including the Counter Registers are initialized to their reset values.

4.2. POWER MANAGEMENT

The circuit is always on and each temperature sensing interval, i.e. every second, is temperature compensated. The digital part is always on, but some functions are clock gated (like I^2C). By default, at power up, the circuit will always go to the lower power consumption mode (power-off). Detecting an activity on the I^2C will wake-up the digital part of the circuit. To achieve the specified time keeping current consumption, extra features like CLKOUT and I^2C interface need to be inactive.

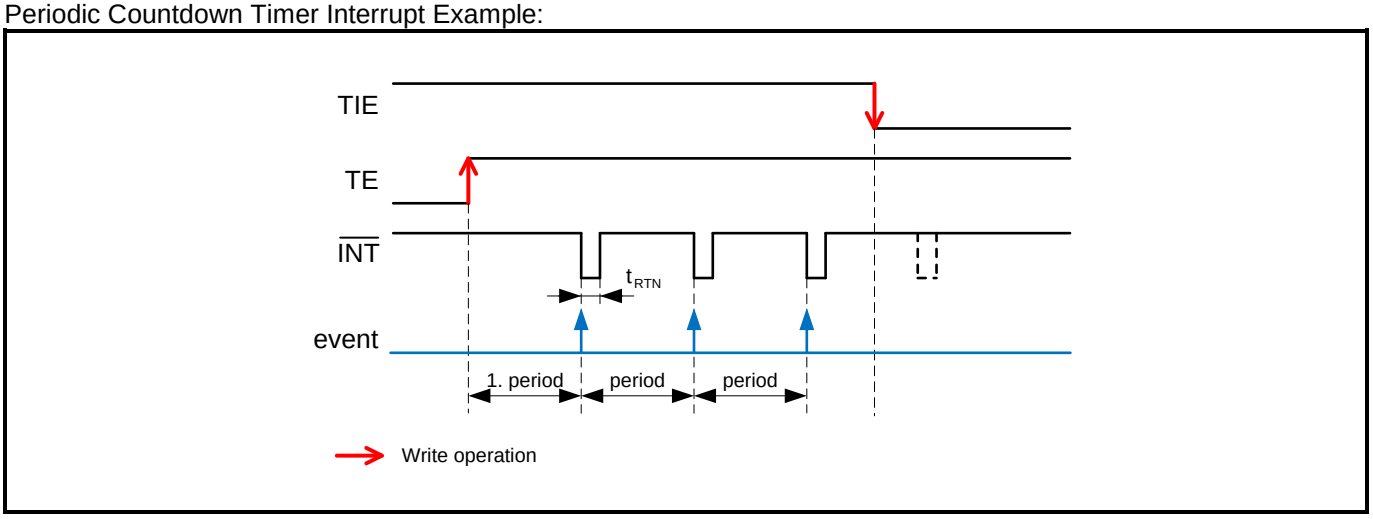
4.3. CLOCK SOURCE

The built-in 32.768 kHz crystal is the clock source for the digital part. After thermal compensation, the RV-8803-C7 provides a very accurate time with temperature compensation for an outstanding low current consumption.

4.4. PERIODIC COUNTDOWN TIMER INTERRUPT FUNCTION

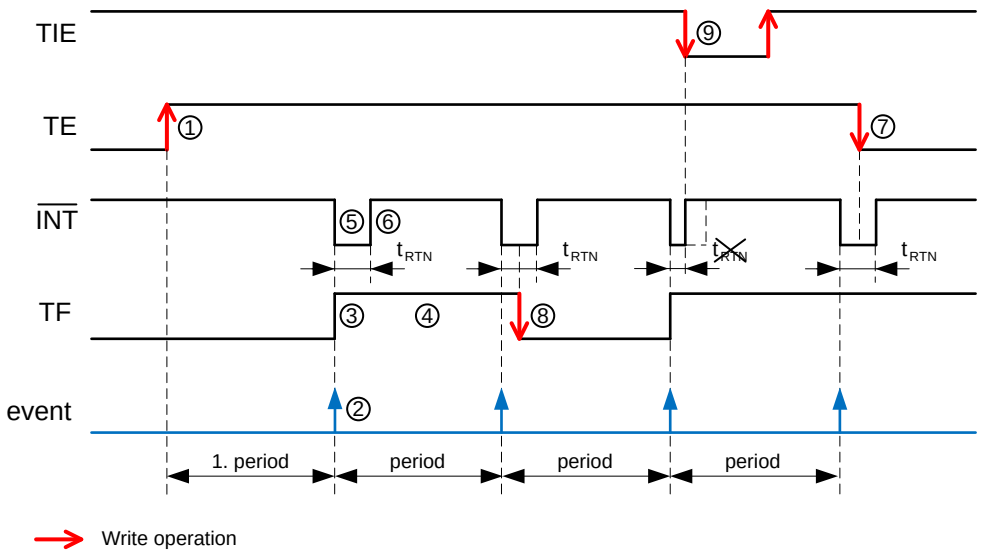
The Periodic Countdown Timer Interrupt function generates an interrupt event periodically at any period set from 244.14 µs to 4095 minutes.
When an interrupt event is generated, the $\overline{INT}$ pin goes to the low level and the TF flag is set to 1 to indicate that an event has occurred. The output on the $\overline{INT}$ pin is only effective if the TIE bit in the Control Register is set to 1. The low-level output signal on the $\overline{INT}$ pin is automatically cleared after the Auto reset time t_{RTN}. t_{RTN} = 122 µs (TD = 00) or t_{RTN} = 7.813 ms (TD = 01, 10, 11).

Periodic Countdown Timer Interrupt Example:



4.4.1.COMPLETE PERIODIC COUNTDOWN TIMER DIAGRAM

Complete Diagram of the Periodic Countdown Timer Interrupt function:



① The Periodic Countdown Timer starts from the preset value when writing a 1 to the TE bit.

② A Periodic Countdown Timer Interrupt event starts a countdown based on the countdown source clock. When the count value reaches 000h, an interrupt event occurs. After the interrupt, the counter is automatically reloaded with the preset value, and starts again the countdown.

③ When a Periodic Countdown Timer Interrupt occurs, the TF bit is set to 1.

④ The TF bit retains 1 until it is cleared to 0 by software.

⑤ If the TIE bit is 1 and a Periodic Countdown Timer Interrupt occurs, the $\overline{INT}$ pin output goes low.

⑥ The $\overline{INT}$ pin output remains low during the Auto reset time t_{RTN}, and then it is automatically cleared to 1. The TD field determines the source frequency and the Auto reset time t_{RTN}.
t_{RTN} = 122 µs (TD = 00) or t_{RTN} = 7.813 ms (TD = 01, 10, 11).

⑦ When a 0 is written to the TE bit, the Periodic Countdown Timer function is stopped and the $\overline{INT}$ pin is cleared after the Auto reset time t_{RTN}.

⑧ If the $\overline{INT}$ pin is low, its status does not change when the TF bit value is cleared to 0.

⑨ If the $\overline{INT}$ pin is low, its status changes as soon as the TIE bit value is cleared to 0.

4.4.2.USE OF THE PERIODIC COUNTDOWN TIMER

The following registers, fields and bits are related to the Periodic Countdown Timer Interrupt function:

- Timer Counter 0 Register (0Bh, 1Bh) (see PERIODIC COUNTDOWN TIMER CONTROL REGISTERS)
- Timer Counter 1 Register (0Ch, 1Ch) (see PERIODIC COUNTDOWN TIMER CONTROL REGISTERS)
- TE bit and TD field (see EXTENSION REGISTER, 0Dh, 1Dh)
- TF bit (see FLAG REGISTER, 0Eh, 1Eh)
- TIE bit (see CONTROL REGISTER, 0Fh, 1Fh)

Prior to entering any timer settings for the Periodic Countdown Timer Interrupt, it is recommended to write a 0 to the TIE and TE bits to prevent inadvertent interrupts on $\overline{INT}$ pin. When the RESET bit value is 1, the Periodic Countdown Timer Interrupt function event does not occur. When the Periodic Countdown Timer Interrupt function is not used, the 2 Bytes of the Timer Counter registers (0Bh, 1Bh and 0Ch, 1Ch) can be used as RAM bytes. The Timer source frequency selection field TD is used to set the countdown period (source clock) for the Periodic Countdown Timer Interrupt function (four settings are possible).

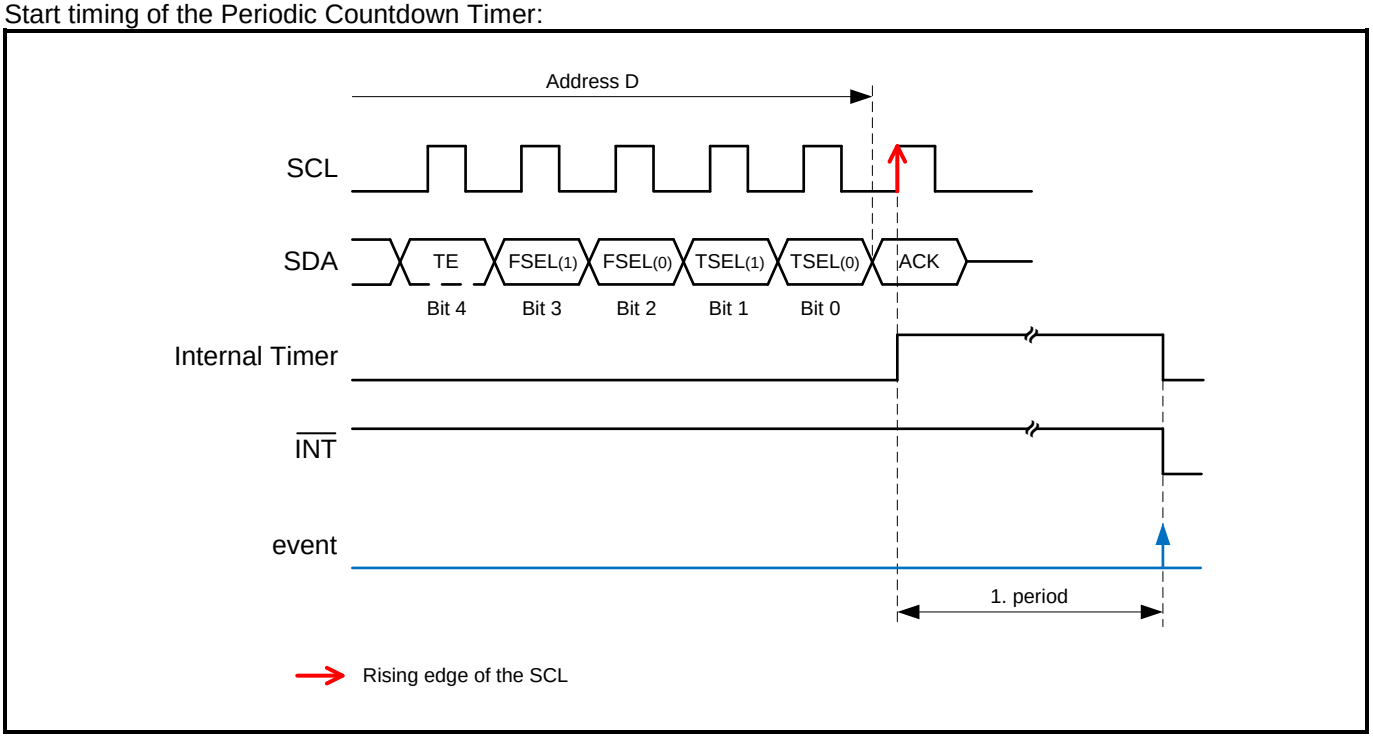
Procedure to use the Periodic Countdown Timer Interrupt function:

1. Initialize bits TIE, TE and TF to 0.
2. Choose the timer source clock and write the corresponding value in the TD field.
3. Choose the interrupt period based on the timer source clock, and write the corresponding preset value to the registers Timer Counter 0 (0Bh, 1Bh) and Timer Counter 1 (0Ch, 1Ch). See following table.
4. Set the TIE bit to 1 if you want to get a hardware interrupt on $\overline{INT}$ pin.
5. Set the TE bit from 0 to 1 to start the Periodic Countdown Timer. The countdown starts at the rising edge of the SCL signal after Bit 0 of the Address D is transferred. The following Figure shows the countdown start timing.

Interrupt period:

Timer counter setting (0Bh, 1Bh), (0Ch, 1Ch)	**Interrupt period**			
	TD = 00 (4.096 kHz)	**TD = 01 (64 Hz)**	**TD = 10 (1 Hz)**	**TD = 11 (1/60 Hz)**
0	-	-	-	-
1	244.14 µs	15.625 ms	1 s	1 min
2	488.28 µs	31.25 ms	2 s	2 min
:	:	:	:	:
41	10.010 ms	640.63 ms	41 s	41 min
205	50.049 ms	3.203 s	205 s	205 min
410	100.10 ms	6.406 s	410 s	410 min
2048	500.00 ms	32.000 s	2048 s	2048 min
:	:	:	:	:
4095 (FFFh)	0.9998 s	63.984 s	4095 s	4095 min

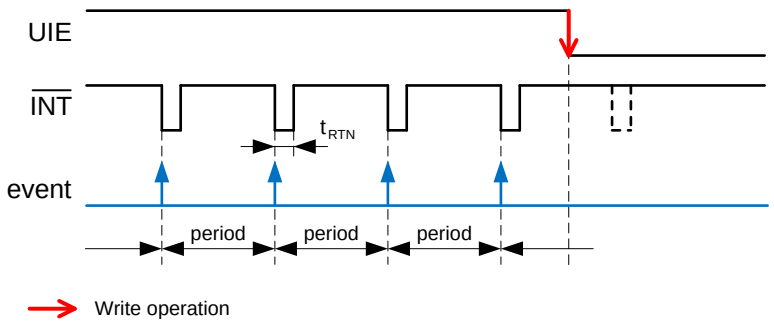
Start timing of the Periodic Countdown Timer:



4.5. PERIODIC TIME UPDATE INTERRUPT FUNCTION

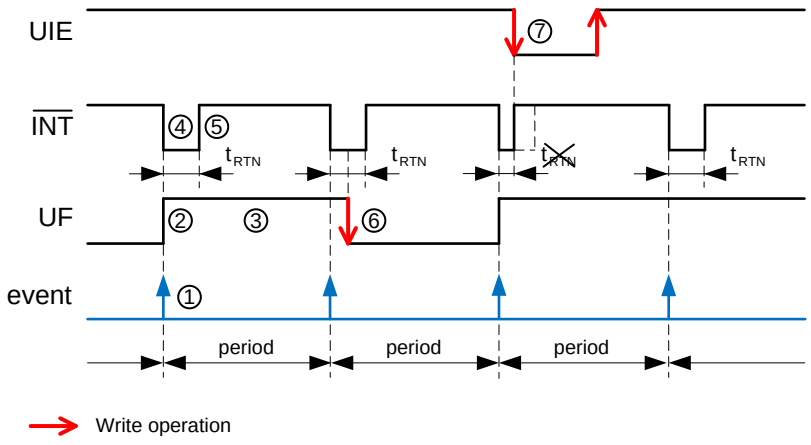
The Periodic Time Update Interrupt function generates an interrupt event periodically at the One-Second or the One-Minute update time, according to the selected timer source with bit USEL.
When an interrupt event is generated, the $\overline{INT}$ pin goes to the low level and the UF flag is set to 1 to indicate that an event has occurred. The output on the $\overline{INT}$ pin is only effective if the UIE bit in the Control Register is set to 1. The low-level output signal on the $\overline{INT}$ pin is automatically cleared after the Auto reset time t_{RTN}. t_{RTN} = 500 ms (Second update) or t_{RTN} = 15.6 ms (Minute update).

Periodic Time Update Interrupt Example:



4.5.1.COMPLETE PERIODIC TIME UPDATE DIAGRAM

Complete Diagram of the Periodic Time Update Interrupt function:



① A Periodic Time Update Interrupt event occurs when the internal clock value matches either the second or the minute update time. The USEL bit determines whether it is the Second or the Minute period with the corresponding Auto reset time t_{RTN}. t_{RTN} = 500 ms (Second update) or t_{RTN} = 15.6 ms (Minute update).

② When a Periodic Time Update Interrupt occurs, the UF bit is set to 1.

③ The UF bit retains 1 until it is cleared to 0 by software.

④ If the UIE bit is 1 and a Periodic Time Update Interrupt occurs, the $\overline{INT}$ pin output goes low.

⑤ The $\overline{INT}$ pin output remains low during the Auto reset time t_{RTN}, and then it is automatically cleared to 1.

⑥ If the $\overline{INT}$ pin is low, its status does not change when the UF bit value is cleared to 0.

⑦ If the $\overline{INT}$ pin is low, its status changes as soon as the UIE bit value is cleared to 0.

4.5.2.USE OF THE PERIODIC TIME UPDATE INTERRUPT

The following bits are related to the Periodic Time Update Interrupt function:

- USEL bit (see EXTENSION REGISTER, 0Dh, 1Dh)
- UF bit (see FLAG REGISTER, 0Eh, 1Eh)
- UIE bit (see CONTROL REGISTER, 0Fh, 1Fh)

Prior to entering any other settings, it is recommended to write a 0 to the UIE bit to prevent inadvertent interrupts on $\overline{INT}$ pin. If the RESET bit is set to 1 (see CONTROL REGISTER, 0Fh, 1Fh) the divider chain is reset and the Periodic Time Update Interrupt function will not be triggered. The reset function only interrupts the Periodic Time Update Interrupt function but does not turn it off.

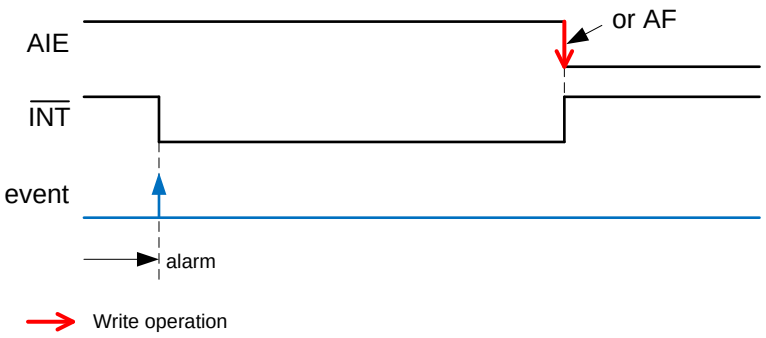
Procedure to use the Periodic Time Update Interrupt function:

1. Initialize bits UIE and UF to 0.
2. Choose the timer source clock and write the corresponding value in the USEL bit.
3. Set the UIE bit to 1 if you want to get a hardware interrupt on $\overline{INT}$ pin.
4. The first interrupt will occur after the next event, either second or minute change.

4.6. ALARM INTERRUPT FUNCTION

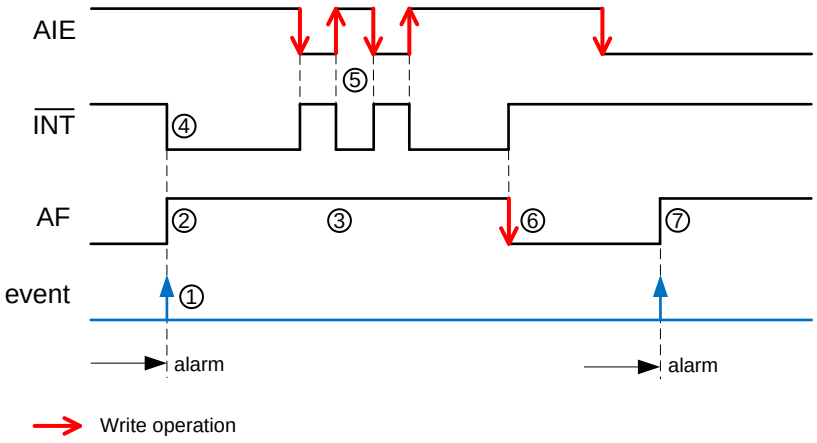
The Alarm Interrupt function generates an interrupt for alarm settings such as date, weekday, hour or minute settings.
When an interrupt event is generated, the $\overline{INT}$ pin goes to the low level and the AF flag is set to 1 to indicate that an event has occurred.

Alarm Interrupt Example:



4.6.1.COMPLETE ALARM DIAGRAM

Complete Diagram of the Alarm Interrupt function:



① A date, weekday, hour or minute alarm interrupt event occurs when the selected Alarm register match the respective counter. The WADA bit determines whether it is the date or weekday.

② When an Alarm Interrupt event occurs, the AF bit value is set to 1.

③ The AF bit retains 1 until it is cleared to 0 by software.

④ If the AIE bit is 1 and an Alarm Interrupt occurs, the $\overline{INT}$ pin output goes low.

⑤ If the AIE value is changed from 1 to 0 while the $\overline{INT}$ pin output is low, the $\overline{INT}$ pin immediately changes its status. While the AF bit value is 1, the $\overline{INT}$ status can be controlled by the AIE bit.

⑥ If the $\overline{INT}$ pin is low, its status changes as soon as the AF bit value is cleared from 1 to 0.

⑦ If the AIE bit value is 0 when an Alarm Interrupt occurs, the $\overline{INT}$ pin status does not go low.

4.6.2.USE OF THE ALARM INTERRUPT

The following registers and bits are related to the Alarm Interrupt function:

- Minutes Register (01h, 12h) (see CLOCK REGISTERS)
- Hours Register (02h, 13h) (see CLOCK REGISTERS)
- Weekday Register (03h, 14h) (see CALENDAR REGISTERS)
- Date Register (04h, 15h) (see CALENDAR REGISTERS)
- Minutes Alarm Register and AE_M bit (08h, 18h) (see ALARM REGISTERS)
- Hours Alarm Register and AE_H bit (09h, 19h) (see ALARM REGISTERS)
- Weekday/Date Alarm Register and AE_WD bit (0Ah, 1Ah) (see ALARM REGISTERS)
- WADA bit (see EXTENSION REGISTER, 0Dh, 1Dh)
- AF bit (see FLAG REGISTER, 0Eh, 1Eh)
- AIE bit (see CONTROL REGISTER, 0Fh, 1Fh)

Prior to entering any timer settings for the Alarm Interrupt, it is recommended to write a 0 to the AIE bit to prevent inadvertent interrupts on $\overline{INT}$ pin. When the RESET bit value is 1, the Alarm Interrupt function event does not occur. When the Alarm Interrupt function is not used, the 3 Bytes of the Alarm registers (08h, 18h; 09h, 19h and 0Ah, 1Ah) can be used as RAM bytes. In such case, be sure to write a 0 to the AIE bit (if the AIE bit value is 1 and the Alarm registers are used as RAM registers, $\overline{INT}$ may change to low level unintentionally).

Procedure to use the Alarm Interrupt function:

1. Initialize bits AIE and AF to 0.
2. Choose the weekday alarm or date alarm by setting the WADA bit.
3. Write the desired alarm settings in registers 08h, 18h to 0Ah, 1Ah. The three alarm enable bits, AE_M, AE_H and AE_WD, are used to select the corresponding register that has to be taken into account for match or not. See the following table.
4. Set the AIE bit to 1 if you want to get a hardware interrupt on $\overline{INT}$ pin.

Alarm Interrupt:

Alarm enable bits			Alarm event
AE_WD	AE_H	AE_M	
0	0	0	When minutes, hours and weekday/date match (once per weekday/date)(1) – Default value
0	0	1	When hours and weekday/date match (once per weekday/date)(1)
0	1	0	When minutes and weekday/date match (once per hour per weekday/date)(1)
0	1	1	When weekday/date match (once per weekday/date)(1)
1	0	0	When hours and minutes match (once per day)(1)
1	0	1	When hours match (once per day)(1)
1	1	0	When minutes match (once per hour)(1)
1	1	1	Every minute(2)

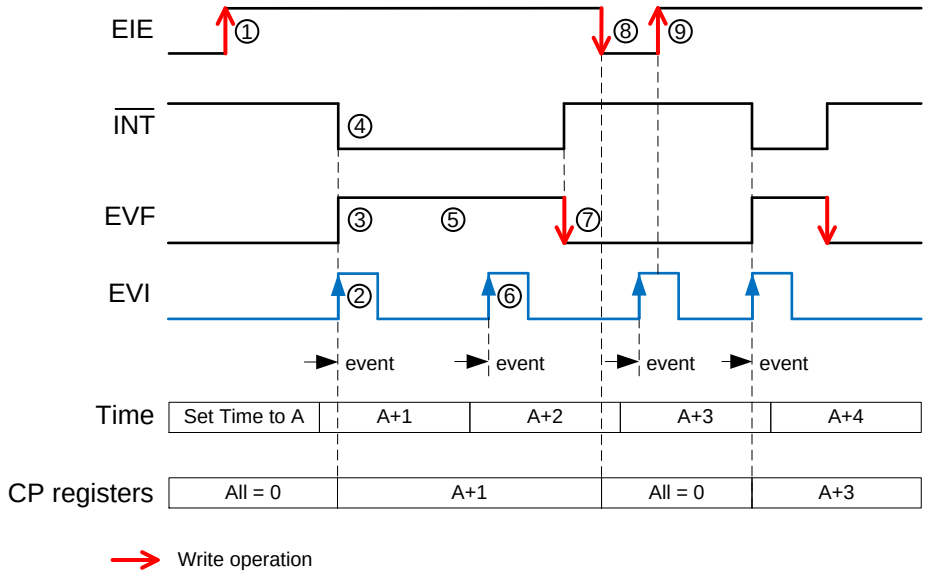
(1) AE_x bits (where x is M, H and WD)
AE_x = 0: Alarm is enabled
AE_x = 1: Alarm is disabled
(2) If all AE_x = 1: Alarm event every minute

4.7. EXTERNAL EVENT FUNCTION

The External Event Interrupt and Time Stamp function is enabled by the control bits EIE and ECP. Depending of the EHL bit a high or low level signal can be regarded as an event and furthermore a digital glitch filtering is applied to the EVI signal when selecting a sampling period in the ET field.
If enabled and an External Event on EVI pin is detected, the seconds and 100th seconds are captured and copied into the Seconds CP and 100th Seconds CP registers, the $\overline{INT}$ is issued and the EVF flag is set to 1 to indicate that an external event has occurred.

4.7.1.COMPLETE EXTERNAL EVENT DIAGRAM

Complete Diagram of the External Event function:



① Initialize time and set EIE bit to 1. The EVF flag need to be cleared to reset the $\overline{INT}$ pin and to prepare the system for an event.
② An External Event on EVI pin is detected. Pay attention to the debounce time when using the filtering.
③ When an External Event Interrupt occurs, the EVF flag is set to 1.
④ If the EIE bit is 1 and an External Event Interrupt occurs, the $\overline{INT}$ pin output goes low.
⑤ The EVF flag retains 1 until it is cleared to 0 by software.
⑥ No interrupt occurs because the EVF flag was not set back to 0. The CP register values do not change.
⑦ If the $\overline{INT}$ pin is low, its status changes as soon as the EVF flag is cleared to 0.
⑧ If the EIE bit value is 0 when an External Event occurs, the $\overline{INT}$ pin status does not go low.
⑨ If the EVI input is 1 (steady state) and the EIE bit is set from 0 to 1 no event is detected.

4.7.2.USE OF THE EXTERNAL EVENT FUNCTION

The following registers and bits are related to the External Event Interrupt function:

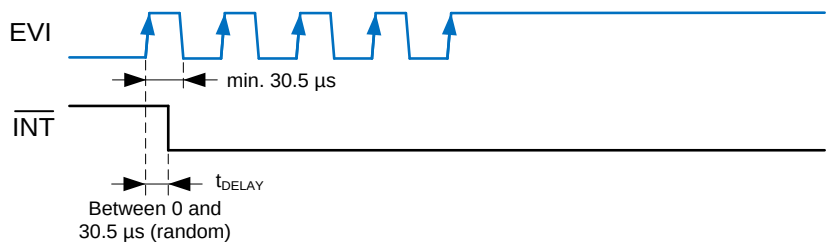
- 100th Seconds Register (10h) (see CLOCK REGISTERS)
- Seconds Register (00h, 11h) (see CLOCK REGISTERS)
- 100th Seconds CP Register (20h) (see CLOCK REGISTERS)
- Seconds CP Register (21h) (see CLOCK REGISTERS)
- ECP bit, EHL bit, ET field and ERST bit (see CAPTURE BUFFER/EVENT CONTROL REGISTERS, 2Fh)
- EVF bit (see FLAG REGISTER, 0Eh, 1Eh)
- EIE bit (see CONTROL REGISTER, 0Fh, 1Fh)

Prior to entering any timer settings for the event interrupt, it is recommended to write a 0 to the EIE bit to prevent inadvertent interrupts on $\overline{INT}$ pin.

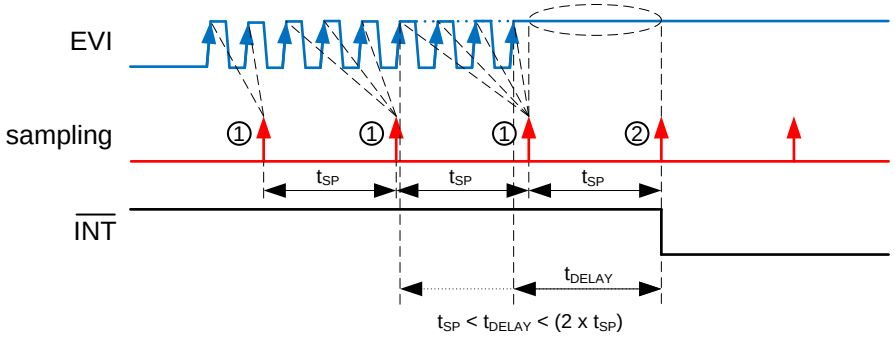
Procedure to use the External Event Interrupt function:

1. Initialize bits EIE and EVF to 0.
2. Set the ECP bit to 1 if you want to capture the seconds and 100th seconds.
3. Set the EHL bit to 1 or 0 to choose high or low level detection on pin EVI
4. Set the ET field to apply filtering to the EVI pin. See following two diagrams.
5. Set the ERST bit to 1 if you want to reset the100th seconds, Seconds CP and 100th Seconds CP registers to 0 in case of an event detection. After the event detection, the ERST bit is reset to 0.
6. Set the EIE bit to 1 if you want to get a hardware interrupt on $\overline{INT}$ pin.

No filtering: ET = 00. Example with positive edge detection:



With digital filtering: ET = 01, 10 or 11 (sampling period t_{SP} = 3.9 ms, 15.6 ms or 125 ms). Example with positive edge/level detection:



① Up to this sampling pulse a positive edge was detected but no steady state.

② If a positive edge was detected and a steady state (high level) was detected between ① and ② the $\overline{INT}$ pin output goes low. The delay time t_{DELAY} varies between t_{SP} and (2 x t_{SP}) depending on the bouncing signal on the EVI pin.

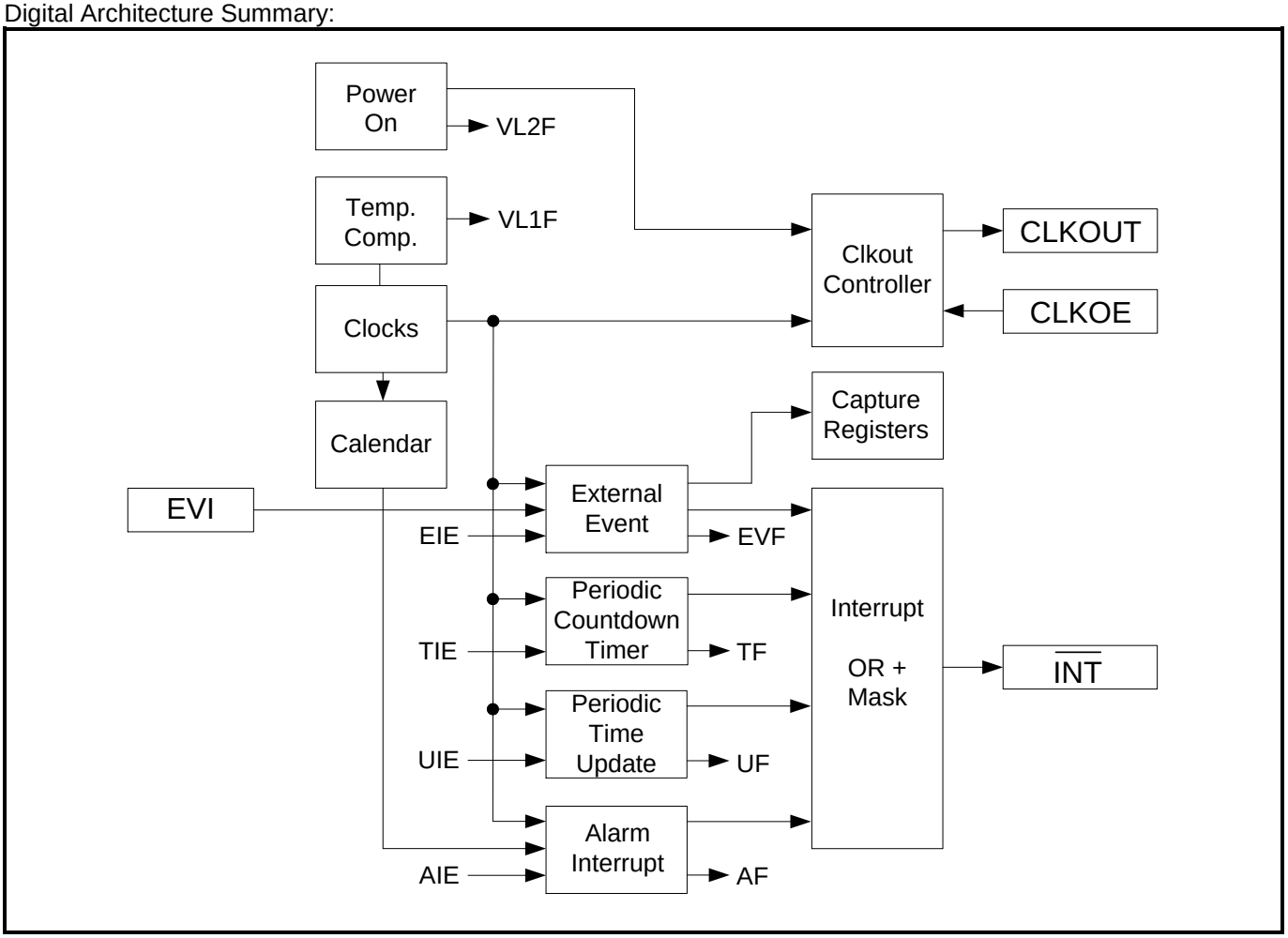
4.8. SERVICING INTERRUPTS

The $\overline{INT}$ pin can indicate four types of interrupts. It outputs the logic OR operation result of these interrupt outputs. When an interrupt is detected, (when the $\overline{INT}$ pin is at low level), the EVF, TF, UF and AF flags can be read to determine which interrupt event has occurred.
To keep the $\overline{INT}$ pin from changing to low level, clear the EIE, TIE, UIE and AIE bits. To check whether an event has occurred without outputting any interrupts via the $\overline{INT}$ pin, software can read the EVF, TF, UF and AF interrupt flags (polling).

4.9. DIGITAL ARCHITECTURE SUMMARY

The following Figure illustrates the overall architecture of the pin inputs and outputs of the RV-8803-C7.

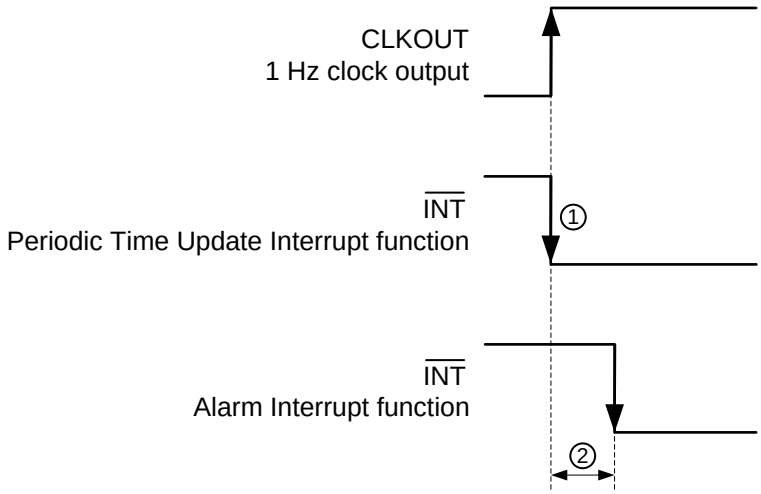
Digital Architecture Summary:



4.10. SYNCHRONICITY BETWEEN $\overline{INT}$ SIGNALS AND 1 HZ CLKOUT

The following Figure illustrates the synchronicity between the $\overline{INT}$ signals from the Periodic Time Update Interrupt function and Periodic Countdown Timer Interrupt function to the 1 Hz CLKOUT signal.

Synchronicity between the $\overline{INT}$ signals and the 1 Hz CLKOUT:



① At the exact same time.
② Delay between 0 and 30.52 µs (random).

4.11. TIME DATA READ-OUT

In order to not corrupt the accuracy of the temperature compensation and the Time Capture function on the highest 100th Seconds resolution, it is not possible to freeze the clock and calendar register during read-out process, as it is common practice for other RTC's.
Since the time and calendar registers cannot be frozen, there might be a condition that the time registers are incremented while read-out. To avoid reading corrupted (partially incremented) data, special measures and procedures need to be applied.

4.11.1. PROCEDURE

The device itself has an automatic function built-in which cuts the I^2C interface after 950 ms to prevent the time and calendar registers from missing internal time increments (see START AND STOP CONDITIONS).

If a time read-out sequence starts at the end of a minute there is a special condition that subsequent registers might be incremented by the time update. To prevent using corrupted data from partially incremented time and calendar registers, it is recommended to repeat and confirm time and calendar data when reading Seconds = 59.

4.11.2. METHODE TO CONFIRM CORRECT TIME AND CALENDAR READ-OUT

When reading Seconds = 59, it is recommended to repeat and compare the read-out of the Seconds register. If the Seconds register data matches, it confirms that the time and calendar data are valid (no time increment occurred during data read-out). If the Seconds value has changed to 00, the second set of time and calendar data is valid.

1. Read required time and calendar information.
2. If Seconds data = 59, a repeated reading is required.
3. If Seconds data is again 59 seconds, then the first data from the first reading is confirmed to be valid.
4. If the Seconds register was incremented (not 59 seconds anymore), then the time and calendar information has been incremented and the second set of data is confirmed to be valid (the first set of data is supposed to be partially incremented during the read-out sequence and therefore is invalid).

5. TEMPERATURE COMPENSATION

5.1. FREQUENCIES

Xtal 32.768 kHz
The Xtal 32.768 kHz clock is not temperature compensated. Due to its negative temperature coefficient with a parabolic frequency deviation, a change of up to -150 ppm across the entire operating temperature range of -40°C to 85°C can result. The oscillator frequency on all devices is tested not to exceed a time deviation of ± 20 ppm (parts per million) at 25°C.

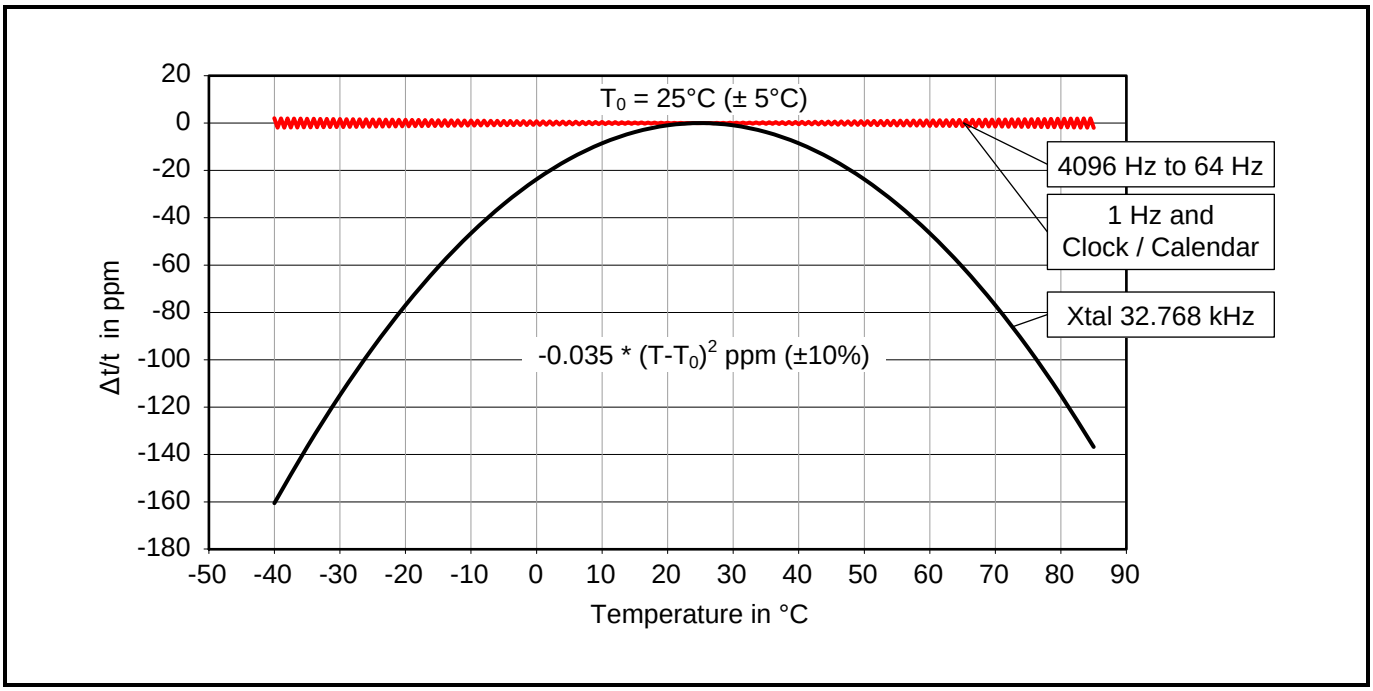
Frequencies from 4.096 kHz to 64 Hz
These frequencies are digitally temperature compensated with a Time Accuracy of +/- 3 ppm over the whole temperature range (-40°C to 85°C). The clock at the 16.384 kHz level of the divider chain is modified by adding or subtracting 32.768 kHz level pulses. The pulses are added or subtracted according to the expected frequency deviation computed by the temperature compensation algorithm. The digital compensation method (adding and subtracting clock pulses) is affecting the cycle-to-cycle jitter of the digitally compensated frequencies shown below.

- 4.096 kHz (Periodic Countdown Timer)
- 1.024 kHz (CLKOUT)
- 100 Hz (External Event Interrupt)
- 64 Hz (Periodic Countdown Timer Interrupt)

Aging compensation can be done with the OFFSET value (see AGING CORRECTION).

1 Hz and Clock / Calendar
The 1 Hz clock is temperature compensated and using both, digital compensation and analog fine adjustment. The Time Accuracy and the Frequency Accuracy is +/- 3 ppm for every 1 Hz period over the whole temperature range (-40°C to 85°C). The temperature compensation algorithm adjusts every 1 Hz period with a resolution of about 0.1 ppm. This precise and accurate 1 Hz clock is used to increment all subsequent clock and calendar registers.
Aging compensation can be done with the OFFSET value (see AGING CORRECTION).

5.2. FREQUENCY VS. TEMPERATURE CHARACTERISTICS



5.3. COMPENSATION VALUES

Each device is factory calibrated over the full temperature range, and the individual compensation values are stored in the EEPROM of the Digital Temperature Compensation Unit (DTCU). The EEPROM is not accessible for the user.

5.4. AGING CORRECTION

An aging adjustment or accuracy tuning can be done with the OFFSET value. The correction is purely digitally and has only the effect of shifting the time vs. temperature curve vertically up or down. It has no effect on the time vs. temperature characteristics of the final frequency. The OFFSET value contains a two's complement number with a range of -2^6 to $+2^6-1$ adjustment steps. The minimal correction step (one LSB) is +/-1/(32768*128) = +/-0.2384 ppm. The maximum correction range is roughly +/-7.4 ppm. Note that the signed offset value OFFSET corresponds to the actual offset value of the measured frequency. The user has access to this field (see OFFSET REGISTER).

The OFFSET value is determined by the following process:

1. Set the OFFSET field to 0 to ensure correction is not occurring.
2. Select the 1 Hz frequency on the CLKOUT pin.
3. Measure the frequency Fmeas at the output pin in Hz.
4. Compute the offset value required in ppm: POffset = ((1 – Fmeas)*1’000’000)
5. Compute the offset value in steps: Offset = POffset/(1/(32768*128)) = POffset/(0.2384)
6. If Offset > 31, the frequency is too high to be corrected.
7. Else if 0 ≤ Offset ≤ 31, set OFFSET = Offset
8. Else if -32 ≤ Offset ≤ -1, set OFFSET = Offset + 64
9. Else the frequency is too low to be corrected.

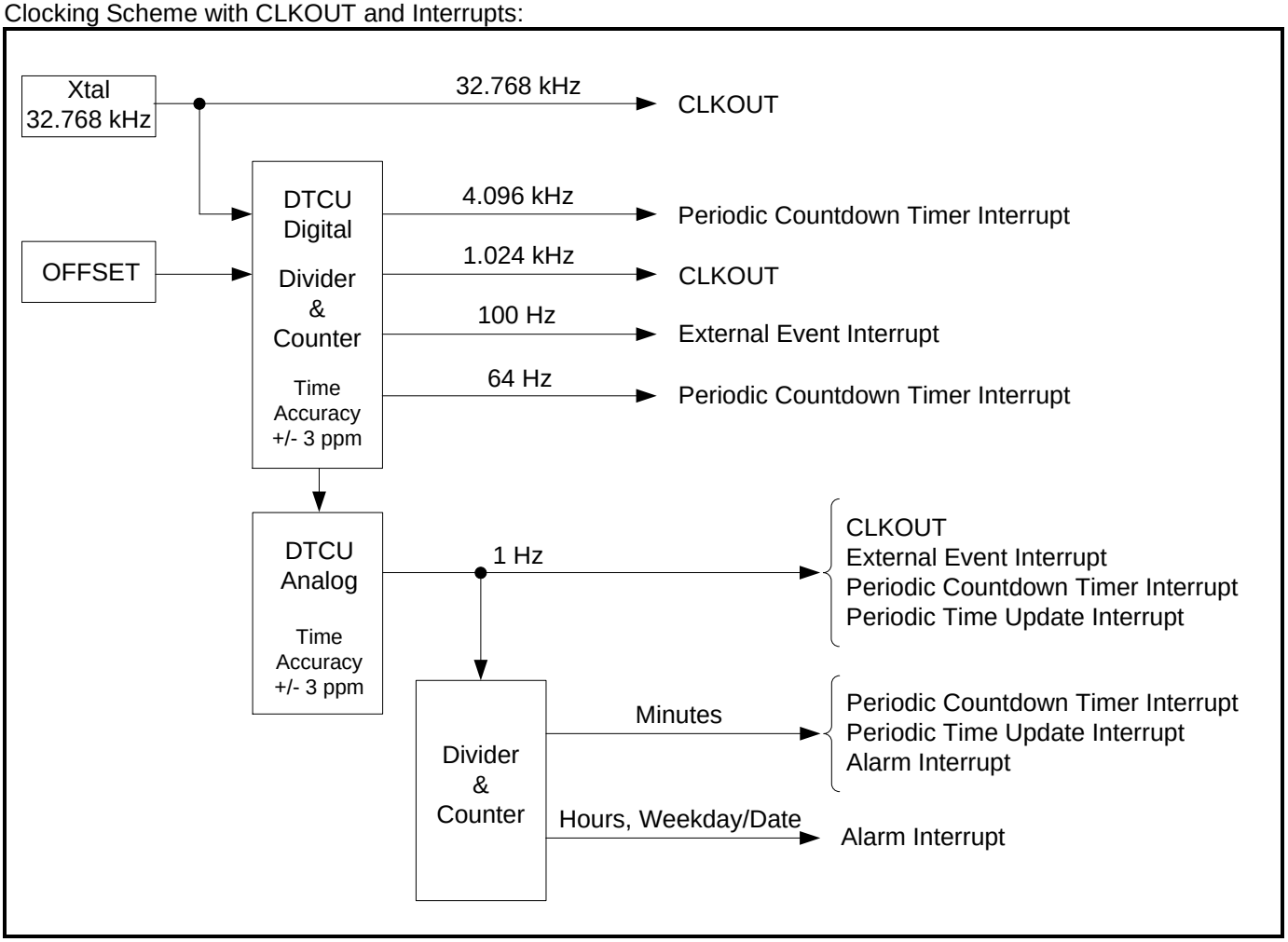
Examples:

- If 1.0000012 Hz is measured when the 1 Hz clock is selected, the offset is +0.0000012 Hz, which is +0.0000012 Hz /·10^{-6} Hz = +1.2 ppm. The positive offset value is then calculated as follows: +1.2 ppm / 0.2384 ppm = +5.03, the rounded integral part is +5. In binary, OFFSET = 000101.

- If 0.9999949 Hz is measured when the 1 Hz clock is selected, the offset is -0.0000051 Hz, which is -0.0000051 Hz /·10^{-6} Hz = -5.1 ppm. The negative offset value is then calculated as follows: -5.1 ppm / 0.2384 ppm = -21.39, the rounded integral part is -21. The unsigned value is then -21 +64 = +43. In binary, OFFSET = 101011.

5.5. CLOCKING SCHEME

Clocking Scheme with CLKOUT and Interrupts:



5.6. MEASURING TIME ACCURACY AT CLKOUT PIN

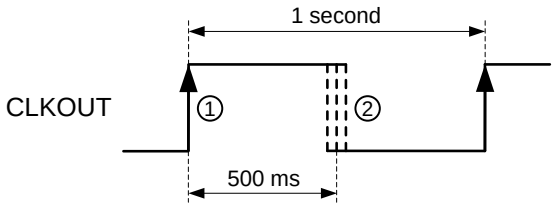
The simplest method to verify the time accuracy of the Digital Temperature Compensation Unit (DTCU) is to measure the compensated 1 Hz frequency at the CLKOUT pin. The 1 Hz clock frequency contains digitally temperature compensation clocks with analog fine adjustment and represents the fully time accuracy of the device.

5.6.1. MEASURING 1 HZ AT CLKOUT PIN

1. Select the 1 Hz frequency at CLKOUT:
   a. Set the FD field to 10 = 1 Hz (see EXTENSION REGISTER, 0Dh, 1Dh).
   b. Set the CLKOUT pin into output mode by setting the CLKOE pin to high level.

2. Measuring equipment and setup:
   a. Use a high-precision universal counter to observe the 1 Hz frequency accuracy on CLKOUT pin.
   b. Trigger on the rising edge of the hybrid signal (gate time ≥ 1 second). Each 1 Hz clock measured at the rising edge fully representing the accuracy of the DTCU.

1 Hz time accuracy at CLKOUT pin (hybrid signal):



① CLKOUT Output is active HIGH.
When measuring the time accuracy it is mandatory to trigger on the rising edge of the CLKOUT signal.
The resolution of the compensated 1 Hz period is about 0.1 ppm (minimal step).

② The falling edge of the CLKOUT signal is generated when the RV-8803-C7 clears the signal after 500 ms.
The negative edge is created by the 32.768 kHz Xtal and must not be used to test the time accuracy.

5.7. MEASURING TIME ACCURACY AT $\overline{INT}$ PIN

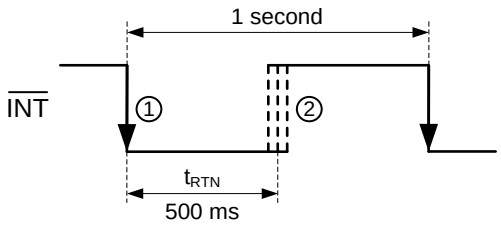
The Periodic Time Update Interrupt function or the Periodic Countdown Timer Interrupt function can also be used to verify the time accuracy of the Digital Temperature Compensation Unit (DTCU) by measuring the compensated 1 Hz frequency at the $\overline{INT}$ output pin. However these two procedures are more sophisticated than using the CLKOUT pin. The following two chapters describe the two methods.

5.7.1. MEASURING 1 HZ WITH THE PERIODIC TIME UPDATE INTERRUPT FUNCTION

1. Select the Periodic Time Update Interrupt function with the frequency 1 Hz at the $\overline{INT}$ output pin:
   a. Write 0 to UIE and UF bits
   b. Choose USEL = 0 = 1 Hz, t_{RTN} = 500 ms (Default value) (see EXTENSION REGISTER, 0Dh, 1Dh)
   c. Set UIE bit to 1 to enable the $\overline{INT}$ pin.
   d. The first interrupt will occur after the next event.

2. Measuring equipment and setup:
   a. Use a high-precision universal counter to observe the frequency stability on $\overline{INT}$ output pin
   b. If measuring the 1 Hz clock it suffices to measure only one period to verify the time accuracy. Trigger on the falling edge of the hybrid signal (gate time ≥ 1 second).

1 Hz time accuracy at $\overline{INT}$ pin with the Periodic Time Update Interrupt function (hybrid signal):



① $\overline{INT}$ Output is active LOW.
When measuring the time accuracy it is mandatory to trigger on the falling edge of the $\overline{INT}$ signal.
The resolution of the compensated 1 Hz period is about 0.1 ppm (minimal step).

② The rising edge of the $\overline{INT}$ signal is generated when the RV-8803-C7 clears the signal after the auto reset time t_{RTN} = 500 ms. The positive edge is created by the 32.768 kHz Xtal and must not be used to test the time accuracy.

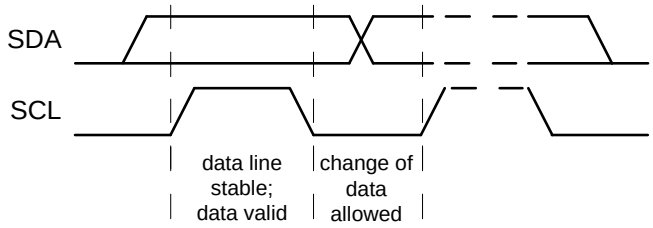
6. I²C INTERFACE

The I²C interface is for bidirectional, two-line communication between different ICs or modules. The RV-8803-C7 is accessed at addresses 64h/65h, and supports Fast Mode (up to 400 kHz). The I²C interface consists of two lines: one bi-directional data line (SDA) and one clock line (SCL). Both lines are connected to a positive supply via pull-up resistors. Data transfer is initiated only when the interface is not busy.

6.1. BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as a control signals. Data changes should be executed during the LOW period of the clock pulse (see Figure below).

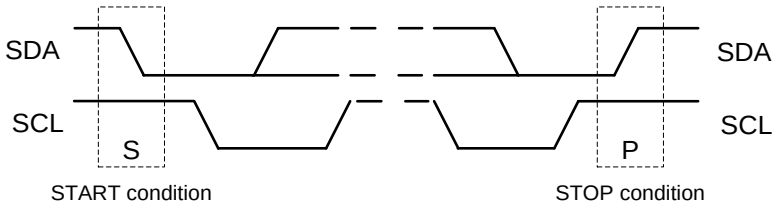
Bit transfer:



6.2. START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see Figure below).

Definition of START and STOP conditions:



A START condition which occurs after a previous START but before a STOP is called a Repeated START condition, and functions exactly like a normal STOP followed by a normal START.

Caution:
When communicating with the RV-8803-C7 module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur **within 950 ms**.

If this series of operations requires **950 ms or longer**, the I²C bus interface will be automatically cleared and set to standby mode by the bus timeout function of the RV-8803-C7 module. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation (when the read operation is invalid, all data that is read has a value of FFh).
Restarting of communications begins with transfer of the START condition again.

6.3. DATA VALID

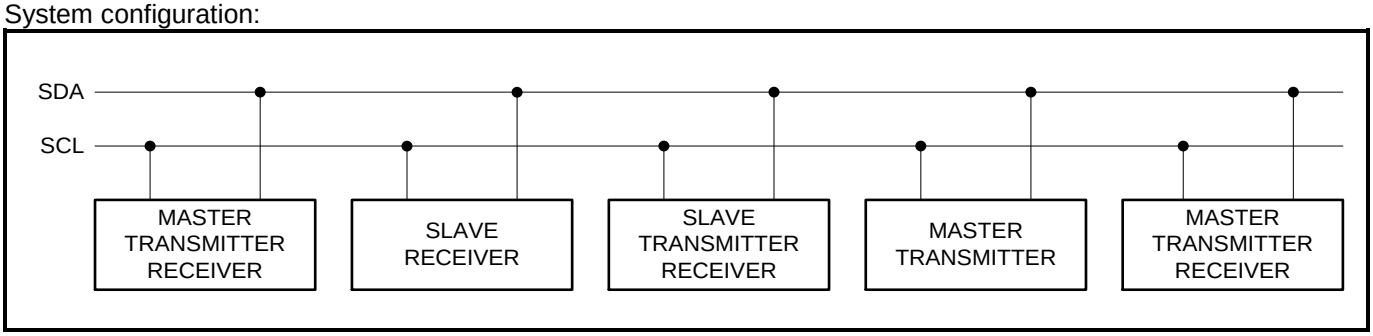
After a START condition, SDA is stable for the duration of the high period of SCL. The data on SDA may be changed during the low period of SCL. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is not limited (however, the transfer time must be no longer than 950 ms). The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

In order to not corrupt the accuracy of the temperature compensation and the Time Capture function on the highest 100th Seconds resolution, it is not possible to freeze the clock and calendar register during read-out process, as it is common practice for other RTC's.
Since the time and calendar registers cannot be frozen, there might be a condition that the time registers are incremented while read-out. To avoid reading corrupted (partially incremented) data, special measures and procedures need to be applied (see TIME DATA READ-OUT).

6.4. SYSTEM CONFIGURATION

Since multiple devices can be connected with the I^{2}C bus, all I^{2}C bus devices have a fixed and unique device number built-in to allow individual addressing of each device.
The device that controls the I^{2}C bus is the Master; the devices which are controlled by the Master are the Slaves. A device generating a message is a Transmitter; a device receiving a message is the Receiver. The RV-8803-C7 acts as a Slave-Receiver or Slave-Transmitter.
Before any data is transmitted on the I^{2}C bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

System configuration:

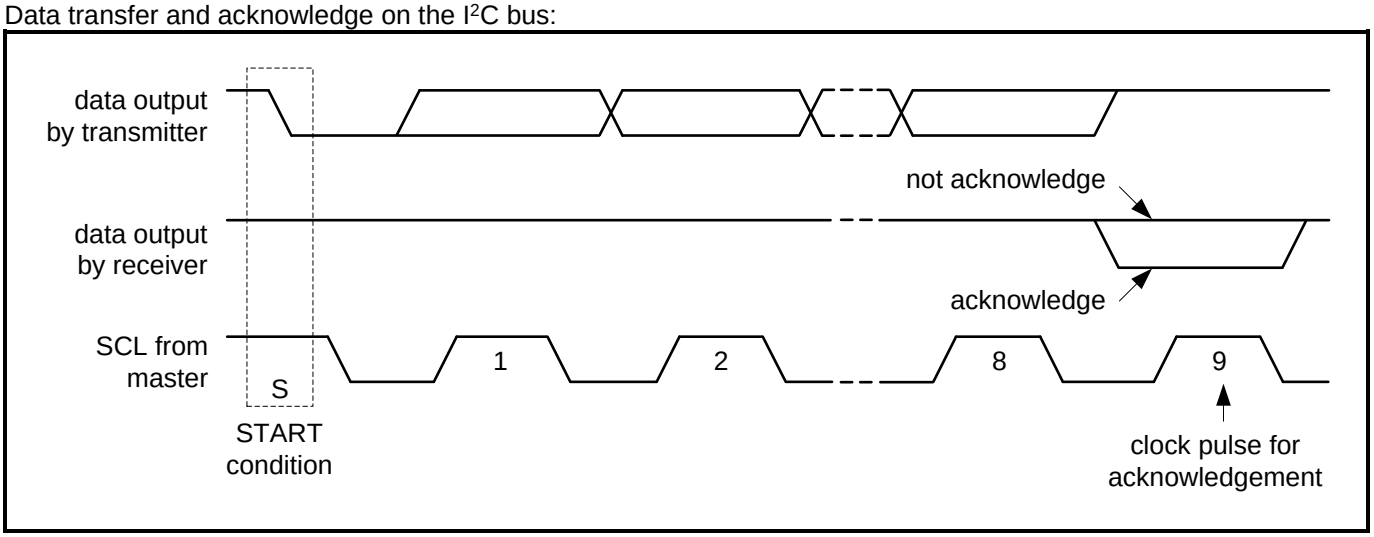


6.5. ACKNOWLEDGE

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited (however, the transfer time must be no longer than 950 ms). Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte.
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Data transfer and acknowledge on the I^2C bus:



6.6. SLAVE ADDRESS

On the I²C bus the 7-bit slave address 0110010b is reserved for the RV-8803-C7. The entire I²C bus slave address byte is shown in the following table.

Slave address							R/$\overline{W}$	Transfer data
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	1	1	0	0	1	0	1 (R)	65h (read)
							0 ($\overline{W}$)	64h (write)

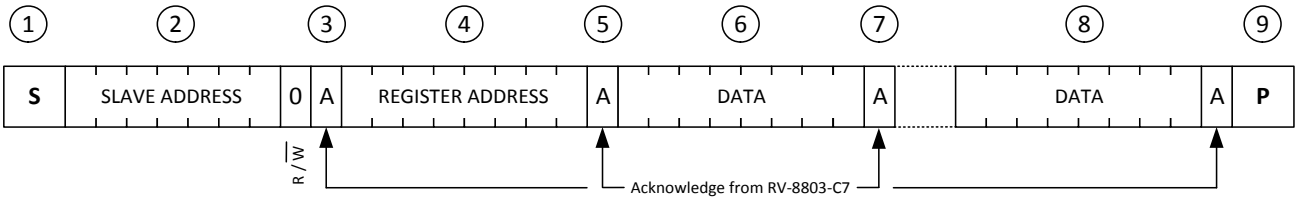
After a START condition, the I²C slave address has to be sent to the RV-8803-C7 device. The R/$\overline{W}$ bit defines the direction of the following single or multiple byte data transfer. The 7-bit address is transmitted MSB first. If this address is 0110010b, the RV-8803-C7 is selected, the eighth bit indicates a read (R/$\overline{W}$ = 1) or a write (R/$\overline{W}$ = 0) operation (results in 65h or 64h) and the RV-8803-C7 supplies the ACK. The RV-8803-C7 ignores all other address values and does not respond with an ACK.
In the write operation, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

6.7. WRITE OPERATION

Master transmits to Slave-Receiver at specified address. The Register Address is an 8-bit value that defines which register is to be accessed next. After writing one byte, the Register Address is automatically incremented by 1.

Master writes to slave RV-8803-C7 at specific address:

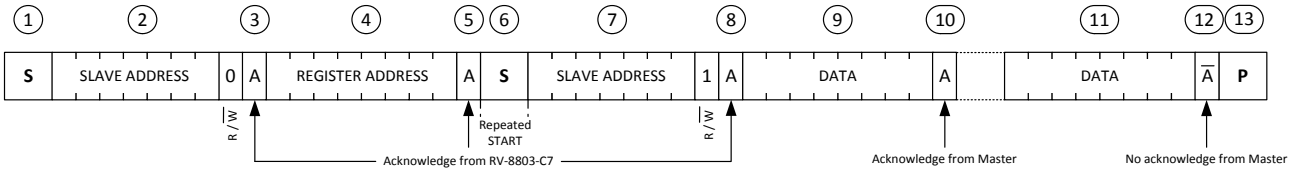
1) Master sends out the START condition.
2) Master sends out Slave Address, 64h for the RV-8803-C7; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-8803-C7.
4) Master sends out the Register Address to RV-8803-C7.
5) Acknowledgement from RV-8803-C7.
6) Master sends out the Data to write to the specified address in step 4).
7) Acknowledgement from RV-8803-C7.
8) Steps 6) and 7) can be repeated if necessary.
   The address is automatically incremented in the RV-8803-C7.
9) Master sends out the STOP Condition.



6.8. READ OPERATION AT SPECIFIC ADDRESS

Master reads data from slave RV-8803-C7 at specific address:

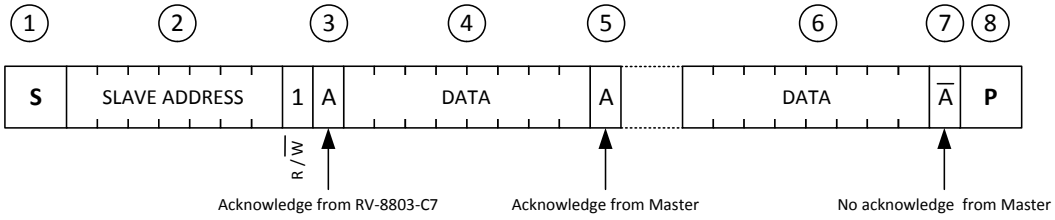
1) Master sends out the START condition.
2) Master sends out Slave Address, 64h for the RV-8803-C7; the R/$\overline{W}$ bit is a 0 indicating a write operation.
3) Acknowledgement from RV-8803-C7.
4) Master sends out the Register Address to RV-8803-C7.
5) Acknowledgement from RV-8803-C7.
6) Master sends out the Repeated START condition (or STOP condition followed by START condition)
7) Master sends out Slave Address, 65h for the RV-8803-C7; the R/$\overline{W}$ bit is a 1 indicating a read operation.
8) Acknowledgement from RV-8803-C7.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
9) The Slave sends out the Data from the Register Address specified in step 4).
10) Acknowledgement from Master.
11) Steps 9) and 10) can be repeated if necessary.
    The address is automatically incremented in the RV-8803-C7.
12) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
13) Master sends out the STOP condition.



6.9. READ OPERATION

Master reads data from slave RV-8803-C7 immediately after first byte:

1) Master sends out the START condition.
2) Master sends out Slave Address, 65h for the RV-8803-C7; the R/$\overline{W}$ bit is a 1 indicating a read operation.
3) Acknowledgement from RV-8803-C7.
   At this point, the Master becomes a Receiver and the Slave becomes the Transmitter.
4) The RV-8803-C7 sends out the Data from the last accessed Register Address incremented by 1.
5) Acknowledgement from Master.
6) Steps 4) and 5) can be repeated if necessary.
   The address is automatically incremented in the RV-8803-C7.
7) The Master, addressed as Receiver, can stop data transmission by not generating an acknowledge on the last byte that has been sent from the Slave-Transmitter. In this event, the Slave-Transmitter must leave the data line HIGH to enable the Master to generate a STOP condition.
8) Master sends out the STOP condition.



7. ELECTRICAL SPECIFICATIONS

7.1. ABSOLUTE MAXIMUM RATINGS

The following Table lists the absolute maximum ratings.

Absolute Maximum Ratings according to IEC 60134:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage		-0.3		6.0	V
V_I	Input voltage	Input Pin	-0.3		V_{DD} +0.3	V
V_O	Output voltage	Output Pin	-0.3		V_{DD} +0.3	V
I_I	Input current		-10		10	mA
I_O	Output current		-10		10	mA
V_{ESD}	ESD Voltage	HBM(1)			±2000	V
		MM(2)			±200	V
I_{LU}	Latch-up Current	Jedec(3)			+/-100	mA
T_{OPR}	Operating Temperature		-40		85	°C
T_{STO}	Storage Temperature		-55		125	°C
T_{PEAK}	Maximum reflow condition	JEDEC J-STD-020C			265	°C

(1) HBM: Human Body Model, according to JESD22-A114.
(2) MM: Machine Model, according to JESD22-A115.
(3) Latch-up testing, according to JESD78., Class I (room temperature), level A (100 mA)

7.2. OPERATING PARAMETERS

For this Table, T_A = -40 °C to +85 °C unless otherwise indicated. V_{DD} = 1.5 to 5.5 V, f_{OSC}= 32.768 kHz, TYP values at 25 °C and 3.0 V.

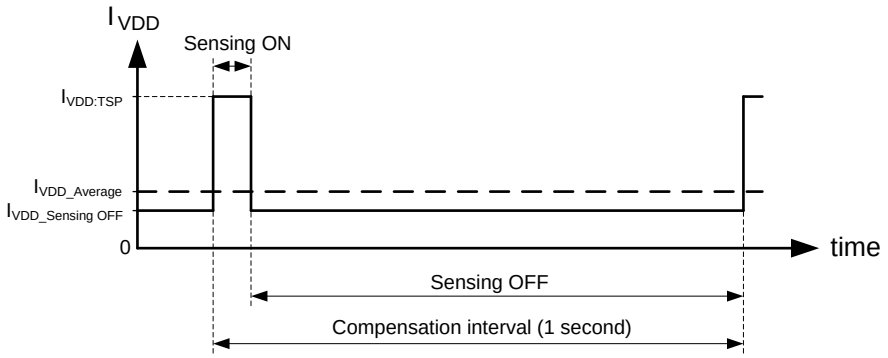
Operating Parameters:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Power Supply Voltage	Time-keeping mode(1)	1.5		5.5	V
		I^2C bus (100 kHz)	1.5		5.5	
		I^2C bus (400 kHz)	2.0		5.5	
V_{LOW1}	V_{DD} low and POR(2) detection. Temperature compensation stops (flag V1F).		1.1	1.2	1.3	V
V_{LOW2}	V_{DD} low and POR(2) detection. Data no longer valid (flag V2F).		1.1	1.2	1.3	V
I_{VDD}	V_{DD} supply current timekeeping. I^2C bus inactive, CLKOUT disabled, average current	V_{DD} = 1.5 V(3)		240	600	nA
		V_{DD} = 3.0 V(3)		240	600	
		V_{DD} = 5.0 V(3)		250	1200	
$I_{VDD:I2C}$	V_{DD} supply current during I^2C burst read/write, CLKOUT disabled	V_{DD} = 1.5 V, SCL = 100 kHz(4)		2	15	µA
		V_{DD} = 3.0 V, SCL = 400 kHz(4)		5	40	
		V_{DD} = 5.0 V, SCL = 400 kHz(4)		7	60	
$I_{VDD:TSP}$	V_{DD} supply current temperature sensing peak	Typical duration = 1.3 ms		19		µA
$I_{VDD:CK32}$	Additional V_{DD} supply current with CLKOUT at 32.768 kHz, average current	V_{DD} = 3.0 V(5)		3.25		µA
$I_{VDD:CK1024}$	Additional V_{DD} supply current with CLKOUT at 1.024 kHz, average current	V_{DD} = 3.0 V(5)		250		nA
$I_{VDD:CK1}$	Additional V_{DD} supply current with CLKOUT at 1 Hz (duty cycle = 500 ms), average current	V_{DD} = 3.0 V(5)		150		nA
Inputs						
V_{IL}	LOW level input voltage	V_{DD} = 1.5 V to 5.5 V Pins: SCL, SDA CLKOE, EVI			0.2 V_{DD}	V
V_{IH}	HIGH level input voltage		0.8 V_{DD}			V
I_{ILEAK}	Input leakage current	$V_{SS} \le V_I \le V_{DD}$	-0.5		0.5	µA
C_I	Input capacitance	V_{DD} = 3.0 V, T_A = 25°C, f = 1MHz			7	pF
Outputs						
$V_{OH:CLK}$	HIGH level output voltage CLKOUT	V_{DD} = 1.5 V, I_{OH} = 0.1 mA	1.2			V
		V_{DD} = 3.0 V, I_{OH} = 1.0 mA	2.5			
		V_{DD} = 5.0 V, I_{OH} = 1.0 mA	4.5			
$V_{OL:CLK}$	LOW level output voltage CLKOUT	V_{DD} = 1.5 V, I_{OL} = -0.1 mA			0.2	V
		V_{DD} = 3.0 V, I_{OL} = -1.0 mA			0.5	
		V_{DD} = 5.0 V, I_{OL} = -1.0 mA			0.5	
V_{OL}	LOW level output voltage Pins: SDA, $\overline{INT}$	V_{DD} = 1.5 V, I_{OL} = -2.0 mA			0.4	V
		V_{DD} = 3.0 V, I_{OL} = -3.0 mA			0.4	
		V_{DD} = 5.0 V, I_{OL} = -3.0 mA			0.3	
I_{OLEAK}	Output leakage current	V_O = V_{DD} or V_{SS}	-0.5		0.5	µA
C_{OUT}	Output capacitance	V_{DD} = 3.0 V, T_A = 25°C, f = 1MHz			7	pF

(1) Clocks operating and RAM and registers retained. Including temperature sensing and compensation.
(2) CLKOUT is hold LOW during the first POR delay t_{POR1} and goes HIGH during the second POR delay t_{POR2}.
(3) All inputs and outputs are at 0 V or V_{DD}.
(4) 2.2k pull-up resistors on SCL/SDA, excluding external peripherals and pull-up resistor current. All other inputs (besides SDA and SCL) are at 0 V or VDD. Test conditions: Continuous burst read/write, 55h data pattern, 25 µs between each data byte, 20 pF load on each bus pin.
(5) All inputs and outputs except CLKOUT are at 0 V or V_{DD}. 10 MΩ, 15 pF load on CLKOUT.

7.2.1.TEMPERATURE COMPENSATION AND CURRENT CONSUMPTION

Typical I_{VDD} average current:



$I_{VDD\_Average}$ = (($I_{VDD:TSP}$ * 1.3 ms) + ($I_{VDD\_Sensing\ OFF}$ * (1 s – 1.3 ms)) / 1 s

$I_{VDD\_Average}$ = ((19 µA * 1.3 ms) + (220 nA * 998.7 ms)) / 1 s = 244 nA

7.3. OSCILLATOR PARAMETERS

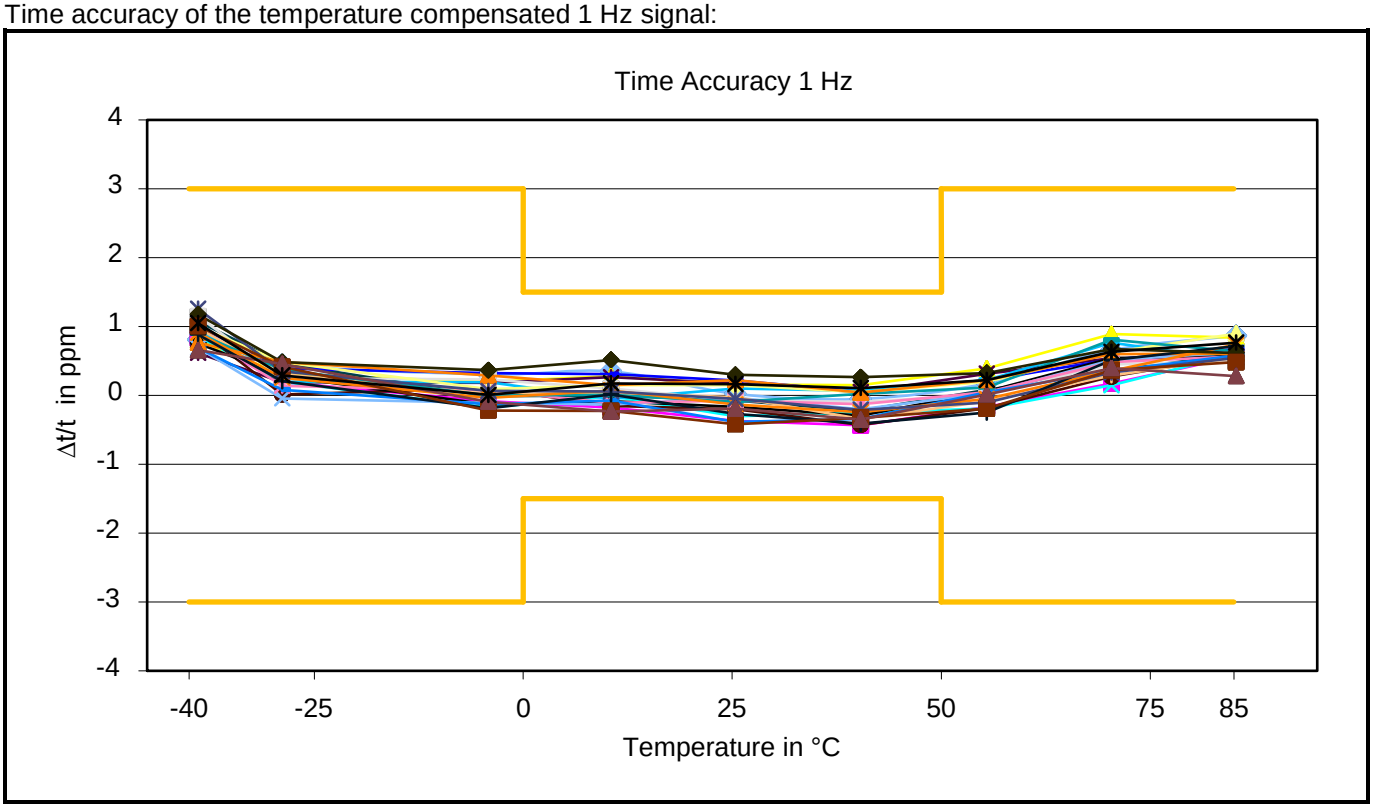
For this Table, T_A = -40 °C to +85 °C unless otherwise indicated. V_{DD} = 1.5 to 5.5 V, f_{OSC}= 32.768 kHz, TYP values at 25 °C and 3.0 V.

Oscillator Parameters:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Xtal General						
F	Crystal Frequency			32.768		kHz
t_{START}	Oscillator start-up time $t_{START} = t_{POR1} + t_{POR2}$	CLKOE = V_{DD}		80	500	ms
δ_{CLKOUT}	CLKOUT duty cycle	F_{CLKOUT} = 32.768 kHz T_A = 25°C		50 ±10		%
Xtal Frequency Characteristics						
ΔF/F	Frequency accuracy	T_A = 25°C, calibration disabled		±10	±20	ppm
$\Delta F/F_{TOPR}$	Frequency vs. temperature characteristics	T_{OPR} = -40°C to +85°C V_{DD} = 3.0 V		$-0.035^{ppm}/_{°C^2}(T_{OPR}-T_0)^2$ ±10%		ppm
T_0	Turnover temperature			+25 ±5		°C
ΔF/F	Aging first year max.	T_A = 25°C, V_{DD} = 3.0 V			±3	ppm
Digital Temperature Compensated Xtal DTCXO						
Δf/f	Time accuracy calibrated, CLKOUT measured on rising edge of One 1 Hz period	T_A = 0°C to +50°C		±1.5		ppm
				±0.13		s/day
		T_A = -40°C to +85°C		±3		ppm
				±0.26		s/day
ΔF/F	1 Hz OFFSET value Min. corr. step (LSB) and Max. corr. range	T_A = -40°C to +85°C	±0.2384		±7.4	ppm

7.3.1.TIME ACCURACY 1 HZ EXAMPLE

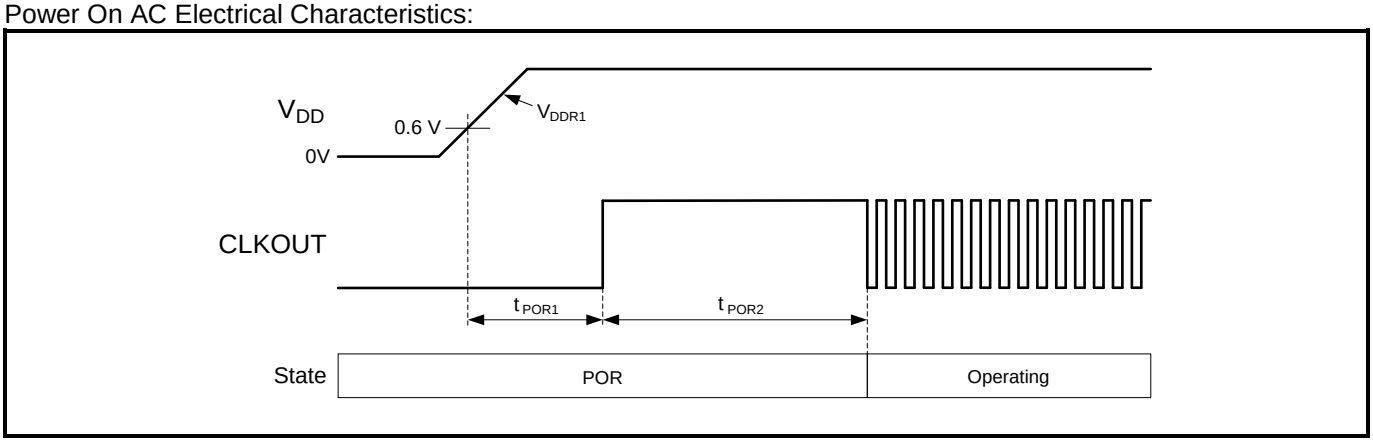
Time accuracy of the temperature compensated 1 Hz signal:



7.4. POWER ON AC ELECTRICAL CHARACTERISTICS

The following Figure and table describe the power on AC electrical characteristics for the CLKOUT pin.

Power On AC Electrical Characteristics:



For this Table, T_A = -40 °C to +85 °C and V_{DD} = 1.5 to 5.5 V, TYP values at 25 °C and 3.0 V.

Power On AC Electrical Parameters:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDR1}	V_{DD} rising slew rate at initial power on reset (POR)	CLKOE = V_{DD}	0.1			V/ms
t_{POR1}	First POR delay			3	10	ms
t_{POR2}	Second POR delay			80	500	ms

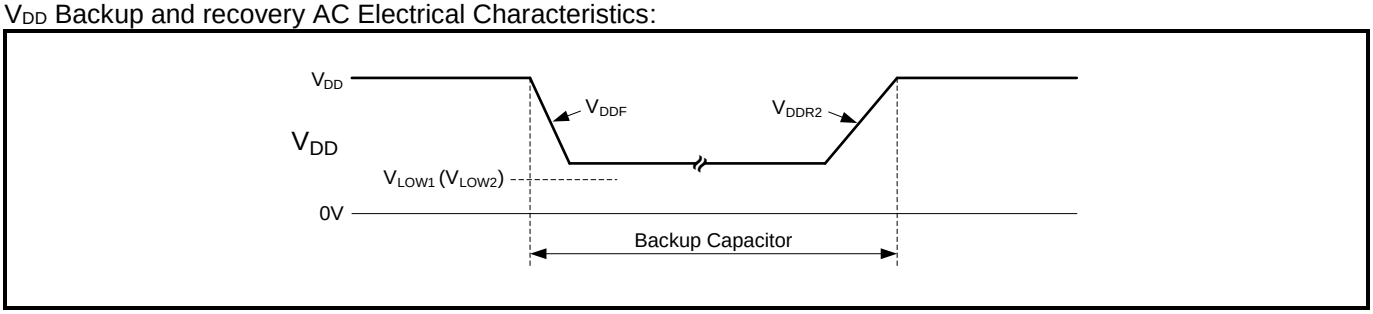
7.5. BACKUP AND RECOVERY

During a backup event with a backup voltage V_{DD} higher than V_{LOW1} (V_{LOW2}) the CLKOUT function is operating including the Temperature compensation and the RAM and registers are retained. Pay attention to the CLKOUT function if the power supply voltage V_{DD} of the RV-8803-C7 sharply goes up and down, meaning V_{DD} is changing between Main power voltage and Backup capacitor voltage. The CLKOUT signal can then disappear for several milliseconds when the voltage change is to sharp.

1. Choose a valid V_{DD} range for the CLKOUT function. E.g. 1.6 V to 3.6 V (see OPERATING PARAMETERS).
2. Ensure that the slew rates V_{DDF} and V_{DDR2} fulfill their specifications.
3. Check if these required specifications are fulfilled on your system.

The following Figure and Table describe the backup and recovery AC electrical characteristics (valid example with a backup voltage > V_{LOW1} (V_{LOW2})).

V_{DD} Backup and recovery AC Electrical Characteristics:



For the following Table, T_A = -40 °C to 85 °C.

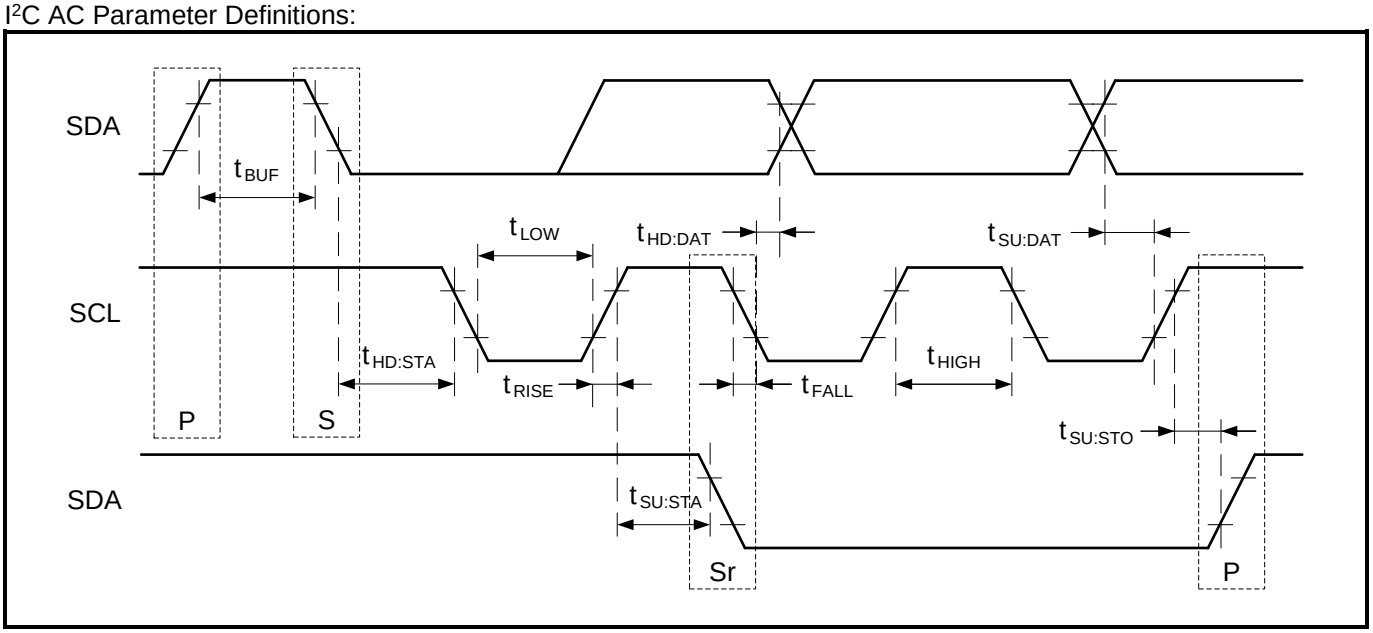
V_{DD} Backup and recovery AC Electrical Parameters:

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDF}	V_{DD} falling slew rate				0.5	V/µs
V_{DDR2}	V_{DD} rising slew rate	Rising from V_{DD} = 1.5 V to $V_{DD} \leq$ 3.5 V			0.2	V/µs
		Rising from V_{DD} = 1.5 V to V_{DD} > 3.5 V			0.07	

7.6. I²C AC ELECTRICAL CHARACTERISTICS

The following Figure and Table describe the I²C AC electrical parameters.

I²C AC Parameter Definitions:



For the following Table, T_A = -40 °C to 85 °C, TYP values at 25 °C.

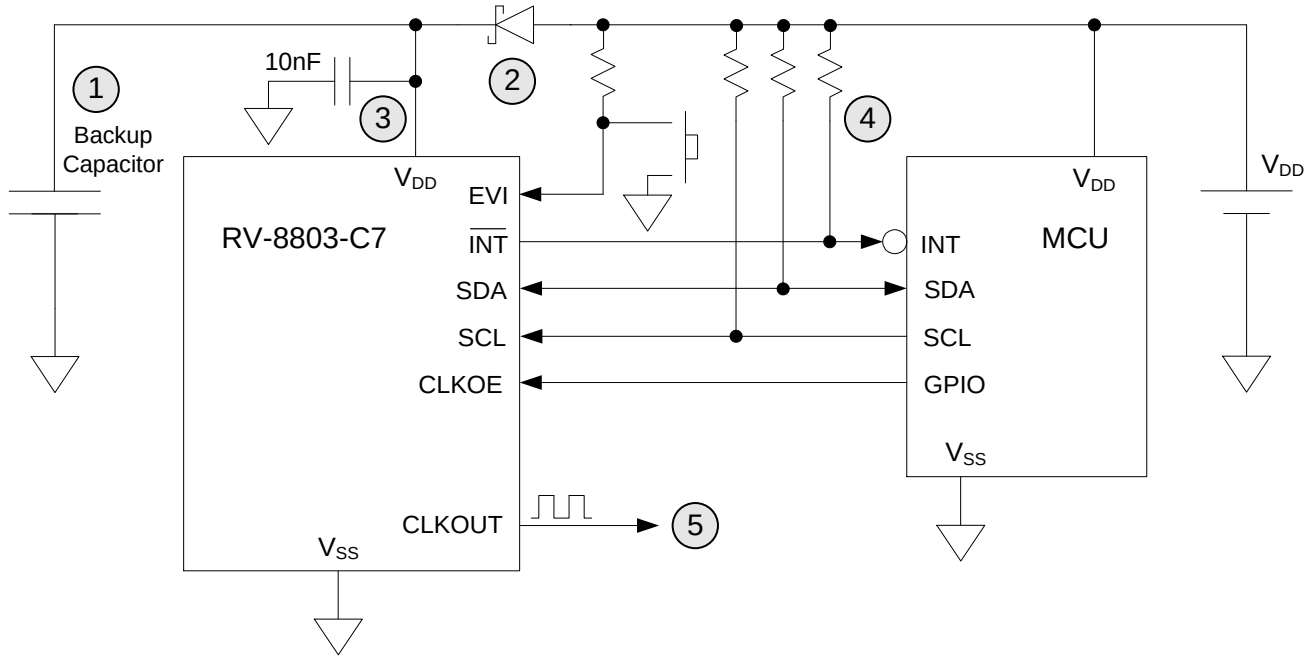
I²C AC Electrical Parameters:

SYMBOL	PARAMETER	Conditions	MIN	TYP	MAX	UNIT
f_{SCL}	SCL input clock frequency	V_{DD} ≥ 1.5 V	0		100	kHz
		V_{DD} ≥ 2.0 V	0		400	
t_{LOW}	Low period of SCL clock	V_{DD} ≥ 1.5 V	4.7			µs
		V_{DD} ≥ 2.0 V	1.3			
t_{HIGH}	High period of SCL clock	V_{DD} ≥ 1.5 V	4.0			µs
		V_{DD} ≥ 2.0 V	0.6			
t_{RISE}	Rise time of SDA and SCL	V_{DD} ≥ 1.5 V			1000	ns
		V_{DD} ≥ 2.0 V			300	
t_{FALL}	Fall time of SDA and SCL	V_{DD} ≥ 1.5 V			300	ns
		V_{DD} ≥ 2.0 V			300	
$t_{HD:STA}$	START condition hold time	V_{DD} ≥ 1.5 V	4.0			µs
		V_{DD} ≥ 2.0 V	0.6			
$t_{SU:STA}$	START condition setup time	V_{DD} ≥ 1.5 V	4.7			µs
		V_{DD} ≥ 2.0 V	0.6			
$t_{SU:DAT}$	SDA setup time	V_{DD} ≥ 1.5 V	250			ns
		V_{DD} ≥ 2.0 V	100			
$t_{HD:DAT}$	SDA hold time	V_{DD} ≥ 1.5 V	0			µs
		V_{DD} ≥ 2.0 V	0			
$t_{SU:STO}$	STOP condition setup time	V_{DD} ≥ 1.5 V	4.0			µs
		V_{DD} ≥ 2.0 V	0.6			
t_{BUF}	Bus free time before a new transmission	V_{DD} ≥ 1.5 V	4.7			µs
		V_{DD} ≥ 2.0 V	1.3			
S = Start condition, Sr = Repeated Start condition, P = Stop condition						

Caution:
When accessing the RV-8803-C7, all communication from transmitting the Start condition to transmitting the Stop condition after access should be completed within 950 ms.
If such communication requires 950 ms or longer, the I²C bus interface is reset by the internal bus timeout function.

8. APPLICATION INFORMATION

8.1. OPERATING RV-8803-C7 WITH BACKUP CAPACITOR

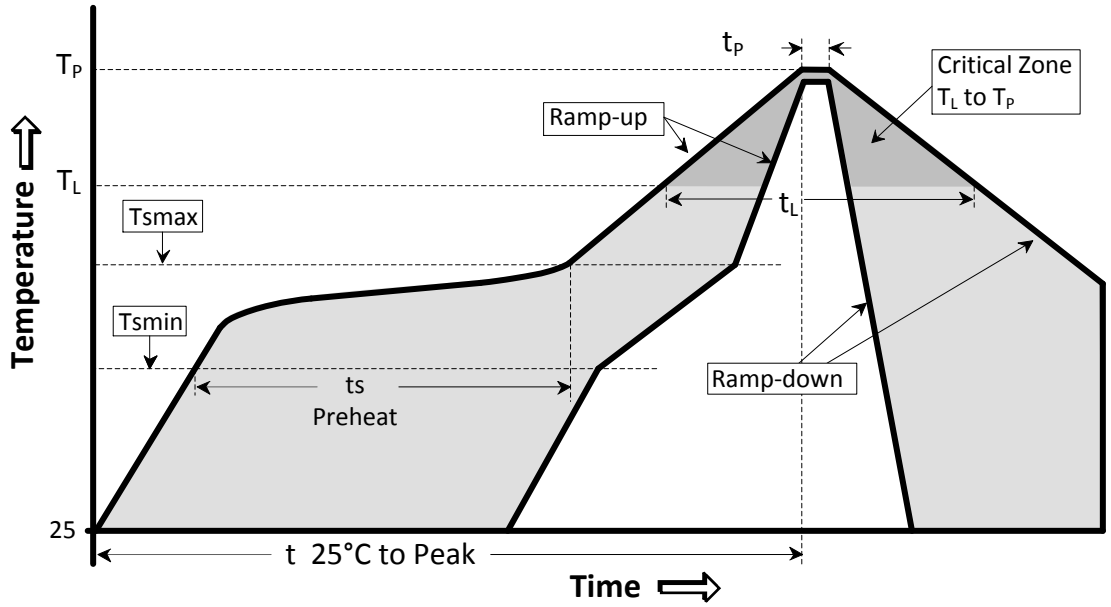


1. Low-cost MLCC (*) ceramic capacitor or supercapacitor.
2. Schottky Diode.
3. A 10 nF decoupling capacitor is recommended close to the device.
4. Interface lines SCL, SDA and the $\overline{INT}$ output are open drain and require pull-up resistors to V_{DD}.
5. CLKOUT offers the selectable frequencies 32.768 kHz, 1.024 kHz and 1 Hz for application use. If not used, it is recommended to disable CLKOUT for optimized current consumption (tie CLKOE to Ground).

(*) Note, that low-cost MLCCs are normally used for short time keeping (minutes) and the more expensive supercapacitors for a longer backup time (day).

9. RECOMMENDED REFLOW TEMPERATURE (LEADFREE SOLDERING)

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"



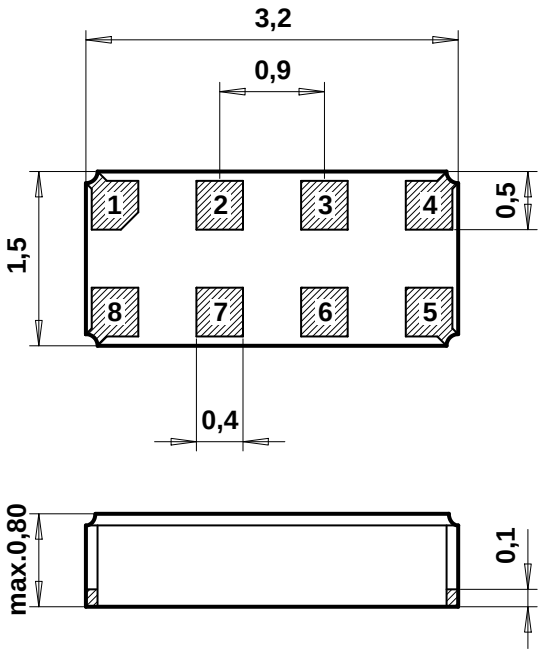
Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	(Ts_{max} to T_P)	3°C / second max	°C / s
Ramp down Rate	T_{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	min
Preheat			
Temperature min	Ts_{min}	150	°C
Temperature max	Ts_{max}	200	°C
Time Ts_{min} to Ts_{max}	ts	60 – 180	sec
Soldering above liquidus			
Temperature liquidus	T_L	217	°C
Time above liquidus	t_L	60 – 150	sec
Peak temperature			
Peak Temperature	Tp	260	°C
Time within 5°C of peak temperature	tp	20 – 40	sec

10. PACKAGE

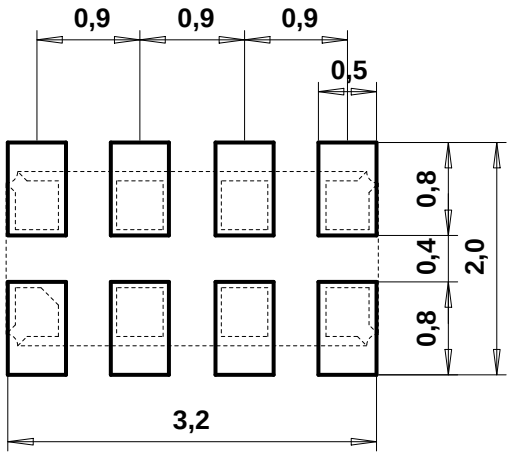
10.1. DIMENSIONS AND SOLDER PAD LAYOUT

C7 Package:

Package dimensions (bottom view):



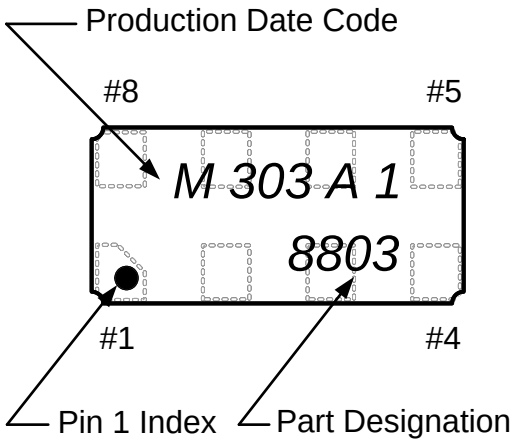
Recommended solder pad layout:



All dimensions in mm typical.

10.2. MARKING AND PIN #1 INDEX

C7 Package: (top view)

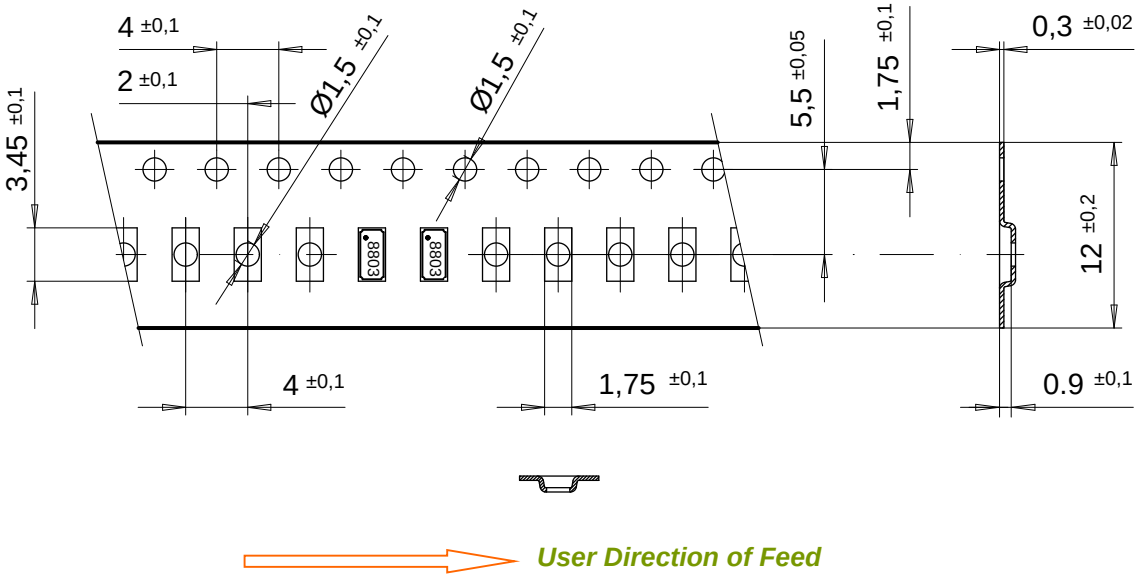


11. PACKING INFORMATION

11.1. CARRIER TAPE

12 mm Carrier-Tape:	Material:	Polystyrene / Butadine or Polystyrol black, conductive
Cover Tape:	Base Material:	Polyester, conductive 0.061 mm
	Adhesive Material:	Pressure-sensitive Synthetic Polymer
	Peel Method:	Middle part removed, sticky sides remain on carrier

C7 Package:



Tape Leader and Trailer: 300 mm minimum.
All dimensions in mm.

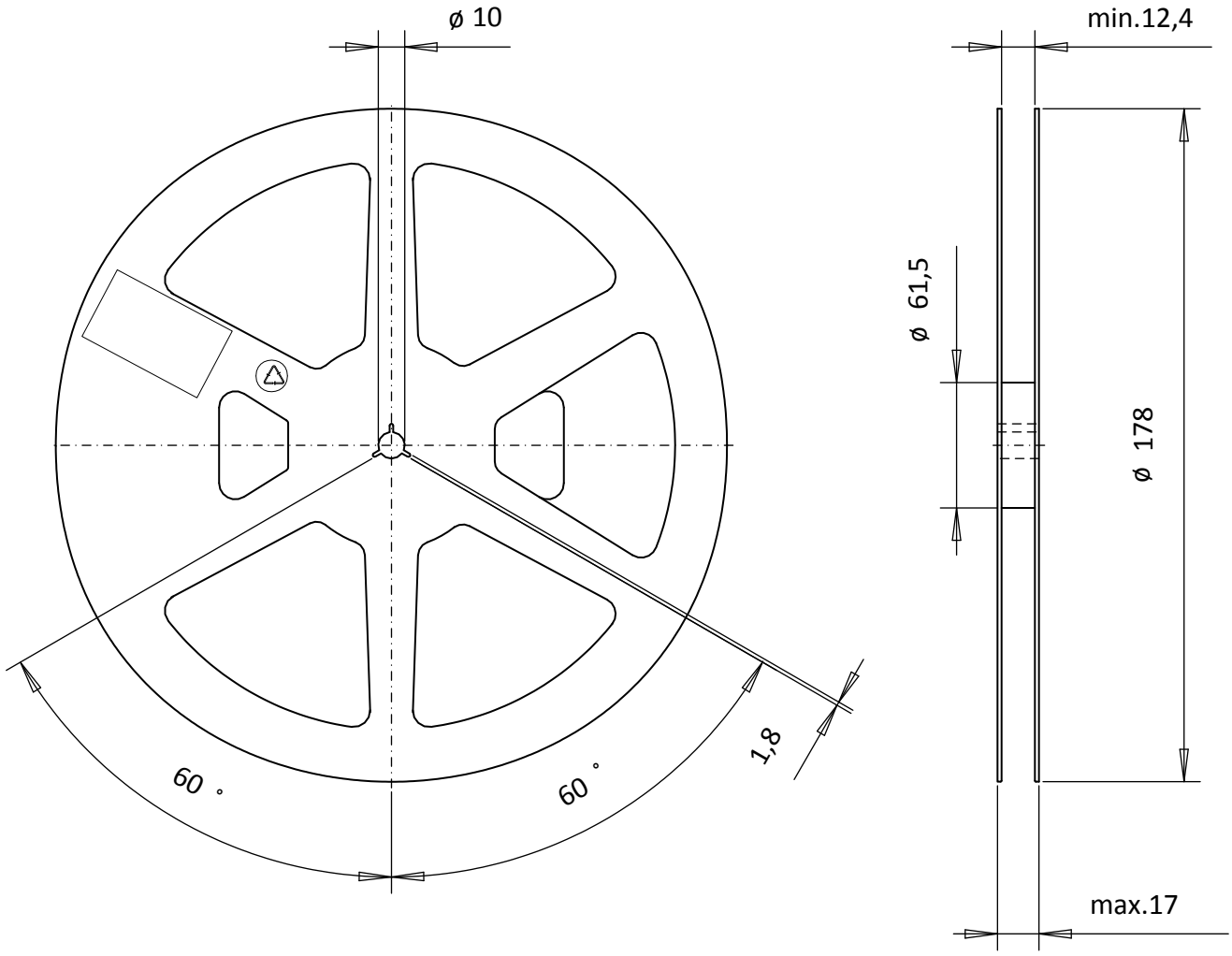
11.2. PARTS PER REEL

C7 Package:

Reels:

Diameter	Material	RTC's per reel
7"	Plastic, Polystyrol	1'000
7"	Plastic, Polystyrol	3'000

11.3. REEL 7 INCH FOR 12 mm TAPE



Reel:

Diameter	Material
7”	Plastic, Polystyrol

11.4. HANDLING PRECAUTIONS FOR CRYSTALS OR MODULES WITH EMBEDDED CRYSTALS

The built-in tuning-fork crystal consists of pure Silicon Dioxide in crystalline form. The cavity inside the package is evacuated and hermetically sealed in order for the crystal blank to function undisturbed from air molecules, humidity and other influences.

Shock and vibration:

Keep the crystal / module from being exposed to **excessive mechanical shock and vibration**. EM guarantees that the crystal / module will bear a mechanical shock of 5000g / 0.3 ms

The following special situations may generate either shock or vibration:

Multiple PCB panels - Usually at the end of the pick & place process the single PCBs are cut out with a router. These machines sometimes generate vibrations on the PCB that have a fundamental or harmonic frequency close to 32.768 kHz. This might cause breakage of crystal blanks due to resonance. Router speed should be adjusted to avoid resonant vibration.

Ultrasonic cleaning - Avoid cleaning processes using ultrasonic energy. These processes can damages crystals due to mechanical resonance of the crystal blank.

Overheating, rework high temperature exposure:

Avoid overheating the package. The package is sealed with a seal ring consisting of 80% Gold and 20% Tin. The eutectic melting temperature of this alloy is at 280°C. Heating the seal ring up to >280°C will cause melting of the metal seal which then, due to the vacuum, is sucked into the cavity forming an air duct. This happens when using hot-air-gun set at temperatures >300°C.

Use the following methods for rework:

- Use a hot-air- gun set at 270°C.
- Use 2 temperature controlled soldering irons, set at 270°C, with special-tips to contact all solder-joints from both sides of the package at the same time, remove part with tweezers when pad solder is liquid.

12. DOCUMENT REVISION HISTORY

Date	Revision #	Revision Details
January 2015	1.0 / 16-0438	First release