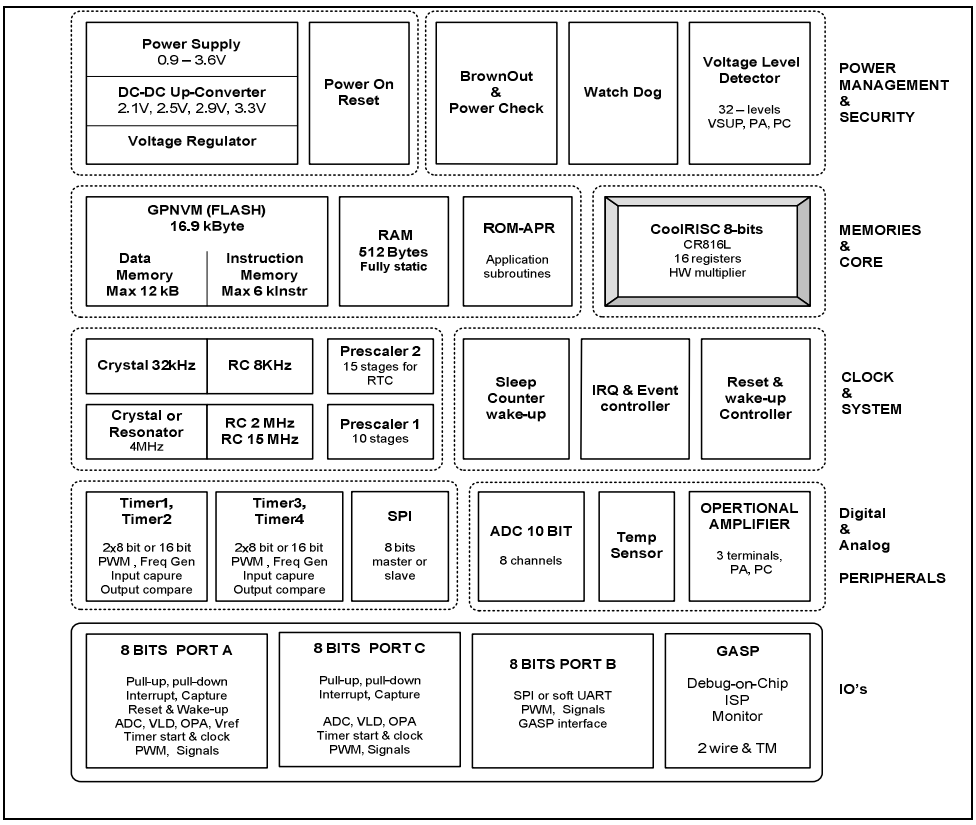
# Ultra Low Power 8 bit Flash µController:

## 0.9V supply, DC-DC Converter, ADC, OpAmp, EEPROM, 8 to 32 leads




## Features

| | |
|---|---|
| **Low Power:** | 140µA @ 3V, Active Mode, CPU: RC_2MHz (1 MIPS)<br>14 µA @ 3V, Standby mode CPU: RC_2MHz<br>2.3 µA @ 3V, Standby mode at 32kHz XTAL<br>1.9 µA @3V, Sleep mode (No clock)<br>0.4 µA @3V, power down mode (Reset state) |
| **Voltage range:** | 0.9V to 3.6V, internal voltage regulator |
| **DC-DC Converter** | Built-IN DC-DC Converter for min 40mA load from VBAT=0.9V |
| **Internal RC Oscillator** | 2MHz and 15MHz, factory pre-trimmed |
| **External Oscillator** | 32'768 Hz watch type crystal or typ 4MHz Resonator |
| **CPU 8 bit** | CR816 Harvard RISC Architecture, 16 Registers, HW multiplier |
| **RAM** | fully static SRAM, 512 Bytes |
| **Flash/EEPROM** | 16.9kByte Flash memory, shared between<br>❑ max 6k Instructions program memory (16.9kByte)<br>❑ max 12k Byte non volatile data memory |
| **Doc** | Debug on chip DoC including In-System Programming |
| **In/Out** | 24 multipurpose I/O's, shared with; SPI, DoC, ADC channels, OpAmp, Vref, Xtal |
| **Timer** | 4 x 8-bit timers (or 2 x 16-bit), 4 x PWM, Freq gen, Capture, Compare |
| **Sleep Counter Reset** | automatic wake-up from sleep mode (EM patent) |
| **Prescaler** | 2 clock prescalers for the peripheral clock generation |
| **IRQ/Events** | on PortA/PortC inputs, Prescaler, Timer, ADC, SPI, Comp |
| **Watchdog** | logic watchdog with dedicated low freq oscillator |
| **VLD** | Voltage Level Detector on Supply and input pin (32 levels) |
| **Brown Out** | Brownout Detection & Start-Up Power check |
| **ADC** | 8 channels 10bits ADC – up to 100kbps |
| **Reference** | pre-trimmed voltage reference output available |
| **Operational Amplifier** | 3 terminal standalone Operational Amplifier or Comparator |
| **Temp. Sensor** | fully internal temperature Sensor |
| **Package** | SOP8, TSSOP16/20/24/28, QFN20/32 (ask for availabiliy) |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**Power supply**
- Low power architecture
- Voltage regulator for internal logic supply
- External regulator capacitor
- **Voltage mult**: gives internal multiplied voltage to allow 0.9V start-up (Padring remains on low-volt)
- **DC-DC Converter**: with ext Coil and Cap. Increases the VBAT for the whole circuit I.e to 3.3V.

**CPU**
- 8-bit CoolRisc 816L Core
- 16 internal registers
- 4 hardware subroutine stacks
- 8-bit hardware multiplier
- refer also to the CR816L reference manual

**Flash/EEPROM**
- 16.9k Byte shared Genaral Purpose Non Volatile Flash memory
- max 6k Instructions program memory
- max 12 kByte non volatile data memory

**RAM**
- 512 x 8-bit static SRAM
- 48 byte of Ram-Cash for EEPROM modification support

**Operating modes**
- **Active mode**: CPU and peripherals are running
- **Standby mode**: CPU halted, peripherals on
- **Sleep mode**: no clocks, data retained
- **Power down** mode, Reset state
  Wake Up Event from PortA inputs

**Resets**
- Power On Reset
- Reset from logic watchdog
- Brown out (as voltage supervisory function)
- Reset with Port A selection
- Flags to identify the reset source

**Watchdog timer**
- generation of watchdog reset after time out
- independent low frequency watchdog oscillator

**Oscillator RC**
- internal RC oscillator, 2MHz and 15MHz pre-trimmed
- < 1% frequency deviation over temperature range

**External Oscillator**
- 32 kHz watch type Crystal or 4MHz Resonator

**Prescaler's**
- Pre-division factors for system clocks of 1, 2, 4 or 8x are available, for CPU and prescaler's
- Two clock prescalers (dividers) for the peripheral clock generation:
  - Prescaler 1 is a 15-stage divider
  - Prescaler 2 is a 10-stage divider
- input clock software selectable
- fix intervall IRQ's

**Interrupt**
- external IRQ's from Port A, VLD, Comparator
- internal IRQ's from Timer, Prescaler, ADC, SPI
- Event from SPI/ADC and DoC

**Parallel In/Output Port A, Port C**
- 8-bit wide direct input read
- all functions bit-wise configurable
  - Input , output
  - Debouncer, IRQ on pos. or neg. edge
  - Input combination reset
  - Pullup, pulldown or nopull selectable
  - Freq. Input for timer
  - Analog In/Out

**Parallel In/Output Port B**
- 8 multipurpose I/O's
- 8-bit wide direct input read
- CMOS or Nch. Open Drain outputs
- all functions bit-wise configurable
  - Input , output
  - Pullup, pulldown or nopull selectable
  - CMOS or Nch. Open Drain outputs

**Serial Port Interface SPI**
- 3 wire serial Interface, Sclk, Sin, Sout
- master and Slave mode
- Serial datastream output
- Event / IRQ
- Maped on port outputs

**Timer (4 x 8-bit, or 2 x 16-bit)**
- 8 (16) bit wide, Zero Stop and Auto Reload mode
- External signal pulse width measurement
- PWM generation, IRQ
- Event Counter
- Input capture
- Output compare

**Sleep Counter Reset (SCWUP)**
- Automatically wakes up the circuit from sleep mode
- Enable/disable by register

**VLD**
- Detection of 32 voltage levels (0.8V to 3.0V)
- Source from VSUP, input Pin or Op.Amp output

**Op. Amplifier / Comparator**
- All 3 terminals mapped on PortA/PortC
- Output routed to internal VLD cell
- Amplifier or Comparator output

**Temp. Sensor**
- Fully internal temperature sensor
- Multiplexed input to ADC

**Brown Out**
- On-chip Brown-Out detection, reset state
- Power check at Startup

**ADC**
- 10-bit, 8 channels ADC, up to 100kbps conversion time
- Single or Continuous mode
- Successive approximation register
- External/internal reference voltage available on a pad
- Event / IRQ

**DoC (Debug on Chip)**
- 2 wire serial interface debug and programming interface
- Flash programming
- Event / IRQ


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