Application Note 604005

Title: **U2270B replacement by EM4095 reader chip**

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1. Introduction

This application note introduces a straightforward solution to use the EM4095 as replacement IC of the U2270B Atmel reader chip. EM4095 is a CMOS integrated transceiver circuit for RFID applications working with transponders at a frequency of typically 125 kHz. It integrates a PLL system to achieve self-adaptive carrier frequency to antenna resonant frequency and can communicate with a microprocessor via a simple interface.

This paper describes the main differences between the two ICs and then it focuses on what hardware changes have to be done to pass from an U2270B to an EM4095 hardware design. Finally, helpful design tips are mentioned to get the best performances of the EM4095. A complete technical overview of the EM4095 is presented in the application note 404 which can be downloaded on the webpage of EM Microelectronic RFID Support Tool or simply by clicking here.

2. Key features comparison

2.1. Absolute Maximum Ratings

U2270B

Parameter	Symbol	Conditions
Maximum Voltage at V_S	V_S	8V
Max. Voltage other pads	V_{IN}	V_S + 0.3
Maximum AC peak current on coils	I_{COIL}	200 mA

EM4095

Parameter	Symbol	Conditions
Maximum Voltage at V_{DD}	V_{DD}	V_{SS} + 6V
Max. Voltage other pads	V_{MAX}	V_{DD} + 0.3V
Maximum AC peak current on coils	I_{ANTmax}	300 mA

As EM4095 can stand a higher current at his coils, a stronger magnetic field can be generated which should allow a bigger reading range for an equivalent design.

2.2. Operating Conditions

U2270B

Parameter	Symb	Min	Typ	Max	Units
Operating junction temperature	T_J			150	°C
Supply Voltage	V_S	4.5		6.3	V
Supply Voltage	V_{EXT}, D_{VS}	4.5		8	V
Antenna resonant frequency	F_{RES}	100	125	150	kHz
Package thermal resistor SO16	$R_{th\ j\text{-}a}$		120		°C/W

EM4095

Parameter	Symbol	Min	Typ	Max	Units
Operating junction temperature	T_J	-40		110	°C
Supply Voltage	V_{DD}	4.1	5	5.5	V
Antenna resonant frequency	F_{RES}	100	125	150	kHz
Package thermal resistor SO16	$R_{th\ j\text{-}a}$	69	70	71	°C/W

2.3. Protocol types supported

Protocol Type	EM4095	U2270B
ASK Biphase	Yes	Yes
ASK Manchester	Yes	Yes
FSK1	Yes	Yes
FSK1_a	Yes	Yes
FSK2	Yes	Yes
FSK2_a	Yes	Yes
PSK	No	No

2.4. Data rate supported

The reception filtering of the EM4095 has two poles at 12 and 25 kHz which means that data rates up to 100 RF clock per bit up should be achievable without any changes in the hardware configuration.

3. Typical Hardware Configuration

3.1. Introduction

As mentioned in the product datasheet, most of the applications can be done with one of the following hardware configurations:

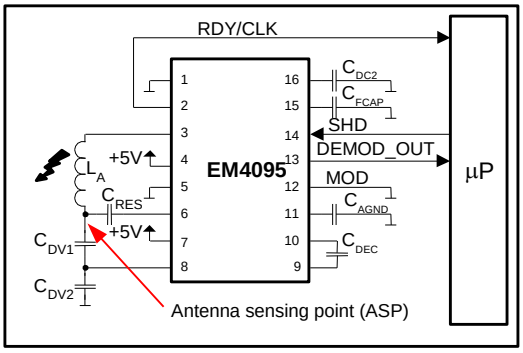

Figure 1 Typical operating configuration for read only mode

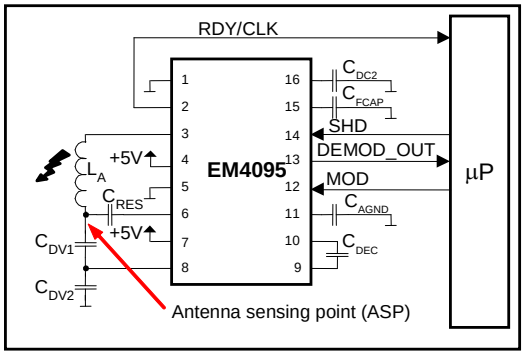

Figure 2 Typical R/W setup using brigde-driver configuration

Typical Component Value:

C_{DC2}	10 nF	C_{AGND}	100 nF // 1nF
C_{FCAP}	10 nF	C_{DEC}	1 nF

C_{RES}, C_{DIV1}, C_{DIV2}, and R_{SER} can be determined thanks to the calculation sheet provided by EM as soon as the value of the inductance $L_{A,}$ is known (you can directly downloaded it by clicking here)

Note that to have good performances of the reader chip we have to paid attention to those specific points:

- Use antenna with Qfactor smaller than 30. If needed, a serial resistor must be added in the resonant circuit.
- Supply carefully the chip (see section 4.2)
- Use an external envelope detector when the internal sensitivity of the IC does not fulfil the application needs (for an increased read range).

3.2. U2270 typical Applications

In the following sections, C_{RES}, C_{DIV1}, C_{DIV2}, and R_{SER} can be determined thanks to the calculation sheet provided by EM as soon as the value of the inductance $L_{A,}$ is known (you can directly downloaded it by clicking here). Moreover, each hardware configuration involving the EM4095 has not been examined for series production or reliability and no worst case scenarios have been developed. Customers who adapts any of these proposals must carry out their own testing and be convinced that no negative consequences arise from the proposals.

3.2.1. Application 1

This application is for intense magnetic coupling only.

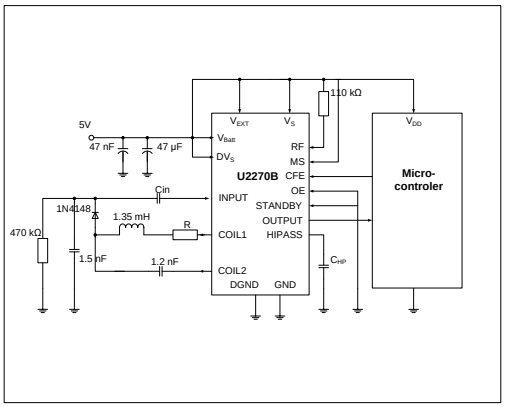

Figure 3 Application using few external components

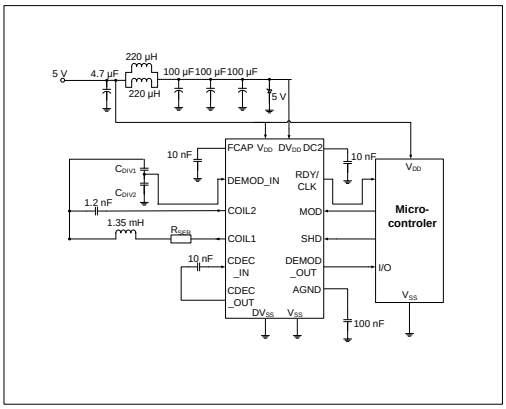

Figure 4 Application using few external components

Note: The use of the external envelop detector is not mandatory for the EM reader chip. The internal demodulation chain must be sufficient to have equivalent read range than the hardware configuration presented in the Figure 3. If an increased read range is needed feel free to add an external envelope demodulator like it is presented in the Figure 6. An example of supply regulation using only passive component is shown in Figure 4. The capacitance divider (CDIV1, CDV2) is used to

reduce the coil voltage at the entrance of the DEMOD_IN pin to a value supported by the reader IC. It must be kept in any cases for the PLL locking.

3.2.2. Application 2

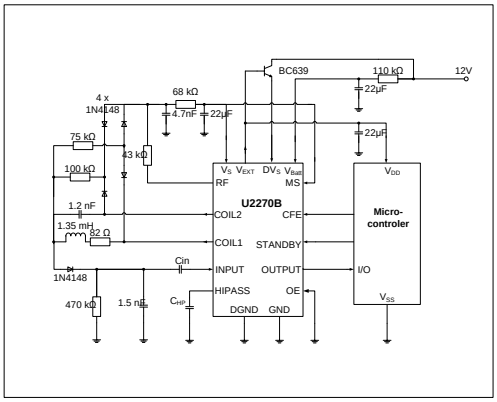

Figure 5 Basic application using diode feedback

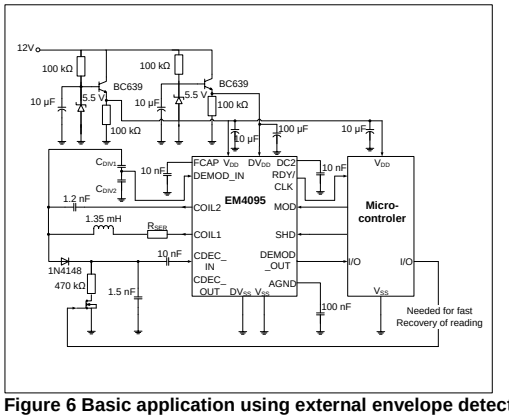

Figure 6 Basic application using external envelope detector and voltage regulation

Note: As said in the section 3.2.1, the use of the external envelop detector is not mandatory for the EM reader chip. Feel free to not use it if an increased read range is not needed. Due to the maximum operating voltage of the EM4095, an example of 12 V supply regulation using active components is shown in Figure 6. Take care to place the decoupling capacitances (electrolytic type of 10 and 100 nF) as close as possible to the pins V_{DD} and DV_{DD} for good performances of the EM4095 (more advices can be found in 4.2 in the Design tips section).

4. Design Tips

Reliability of a reader application using the EM4095 transceiver can be optimized following some basic design rules pointed out in this chapter.

4.1. Board design

Pins DVDD and DVSS should be connected to VDD and VSS respectively. Care should be taken that voltage drops due to driver current which is flowing through pins DVDD and DVSS does not provoke voltage drops on VDD and VSS. The DVSS pin and DVDD pin should be blocked by a 100nF capacitor between the two pins as close as possible to the chip. This should prevent the supply spikes caused by the antenna drivers. Blocking of the analog supply pins VSS and VDD next to the chip is also advisable. Blocking capacitors are not included in the EM4095 application schematics.

All capacitors related to pins DC2, AGND and DMOD_IN should be connected to the same VSS line, which should be connected directly to VSS pin of the chip. This VSS line should not be connected to other elements or be a part of "supply line" going to DVSS.

The interconnecting lines to all the sensitive pins (listed above) must be as short as possible. This is also true for the VSS line to the blocking capacitors. The capacitive coupling from all "hot" lines specially the digital output DEMOD_OUT to the sensitive input pins DEMOD_IN, FCAP, CDEC, DC2 and AGND should be avoided.

EM can provide a sample PCB with EM4095, power supply filter caps and caps on DEMOD_IN, FCAP, CDEC, DC2 and AGND already mounted.

A PCB layout can also be found on EM Microelectronic-Marin SA, in the section RFID Support tool or by clicking here.

4.2. Power supply stability

Since ANT drivers drive antenna with VDD and VSS power supply level it is clear that all variations and noise in power supply are directly fed to antenna resonant circuit. Any supply variation which will result in variation of antenna high voltage in mV region will result in reduced functionality or even malfunction of the system (transponder signal superimposed on antenna voltage is in the range of tens of mV). Special care has to be taken to filter low frequency noise in range up to 20 kHz since the transponder signal is in this frequency range.

4.3. Analog ground pin AGND

The AGND capacitor can be increased from 220nF up to 1uF. The bigger capacitor value can slightly reduce the receive noise. The AGND voltage is filtered by external capacitor and internal resistor of 2kohms.

4.4. Design of DEMOD_IN capacitive divider

Capacitor divider should be designed in a way that parasitic capacitances (few pF of DMOD_IN pin, parasitics of PCB, …) do not influence divider ratio. Capacitor with value from 1 to 2 nF is proposed for connection from DMOD_IN pin to VSS (C_{DV2}). Capacitor from antenna high voltage point to DMOD_IN (C_{DV1}) pin is then calculated from divider ratio.

Additional capacitance of capacitive divider must be compensated by accordingly smaller resonant capacitor.

4.5. Maximum current on ANT driver outputs

EM4095 is not limiting the current delivered by ANT drivers. Absolute maximum rating on these two outputs is 300 mA. Design of antenna resonant circuit connected to ANT drivers must be done in a way that maximum peak current of 250 mA is never exceeded. If quality of antenna is so high that this current might be exceeded, it has to be reduced by adding series resistor. As already mentioned in EM4095 datasheet [1] antenna driver current also defines the maximum operating temperature. Maximum peak current should be designed in a way that internal junction temperature does not exceed maximum junction temperature at maximum application ambient temperature. Based on maximum current and temperature range a choice of packaging has to be done. Low cost package SOIC 16 has Thermal Convection of 70 °C/W and PSOP has 30 °C/W with a special PCB layout (refer to EM4095 Data Sheet).

4.6. Signal MOD

It is recommended to connect MOD to VSS in read-only applications. EM4095 has some built in test features, which are switched on when SHD and MOD pins are high. It is thus recommended that MOD pin is kept low while SHD is high.

4.7. Band pass filter tuning

The reception filtering is done in two stages. The first stage zero is defined by external capacitor Cdec and internal resistor (100 kohms). The pole of the first stage is set internally to ~ 25 kHz. The second stage zero is defined by external capacitor Cdc2 and internal resistor. The pole of the second stage is defined internally to 12 kHz.

This means that the reception poles can not be changed and the upper frequencies are limited by two stages filter having -3dB frequencies at 25 kHz and 12 kHz.

The two stage zeroes can be changed (refer to chapter 4.8 of the Application Note 404).

5. Communicate with Atmel ICs thanks to the demokit EMDB409

Since beginning of December 2012, a software & firmware update of the EMDB409 (EM LF Demokit) can be done. To get the installation files, please contact directly your EMMicrolelectronic contact person (or alternatively by clicking here).

5.1. Chip settings supported

This first software and firmware update supports only tags with some configuration bits enabled: Answer On Request (AOR), Password (PWD), Sequence Terminator (ST) must be enabled. This prerequisite verified, the following options are available to users:

- Encoding: Manchester or Bi-phase
- Bit rate range : RF/16 to RF/128
- Commands : Direct Acces, Regular Read, Write Block, AOR, Change password

5.2. Graphical User Interface (GUI)

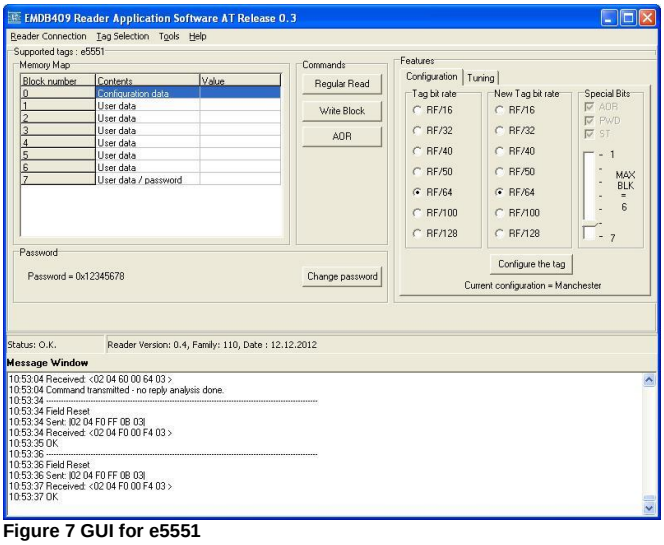

Figure 7 GUI for e5551

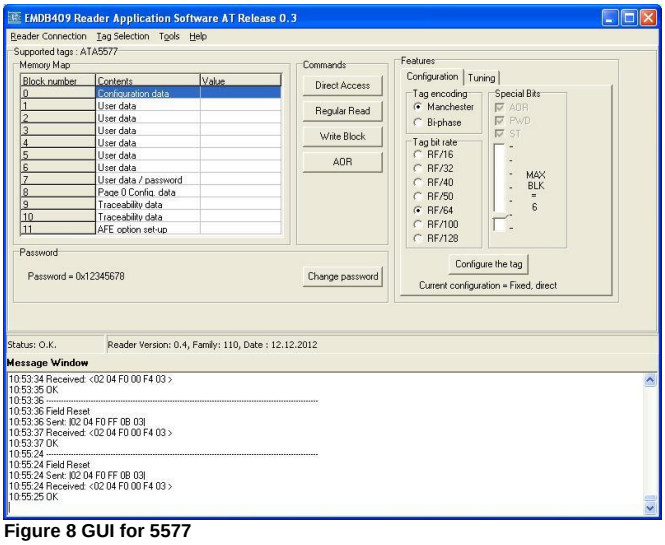

Figure 8 GUI for 5577