POWER MANAGEMENT CONTROLLER WITH ENERGY HARVESTING INTERFACE

Description

The EM8504 is an integrated power management solution for low power applications. It is specifically designed for efficient operation with Dye-Sensitized Solar Cells (DSSC) in the µW to mW range.

To optimize harvesting efficiency, the EM8504 incorporates a maximum power point tracking (MPPT) controller based on a fixed Voltage at Maximum Power Point (VMPP).

The device is designed to speed-up system start-up time when the main energy storage element (aka Long Term Storage – LTS) is completely discharged or insufficiently charged to supply the application, by using a secondary energy storage element (Short Term Storage - STS).

When using a non-rechargeable primary battery the EM8504's on-board PMU offers a mechanism to extend battery life when assisted by a harvesting element.

The EM8504 incorporates a boost converter able to start with an input voltage as low as 300 mV and an input power of few µW.

In functional mode the EM8504 operates at energy levels from a DC harvesting source as low as 100 mV and 1 µW. To maximize harvesting efficiency the EM8504 uses an external voltage to track the maximum power point.

The EM8504 is capable of working with a variety of energy elements as secondary storage, namely re-chargeable batteries, super-capacitors or conventional capacitors. In all cases the EM8504 maintains its fast start-up capability that depends only on the harvester conditions and the STS capacitor value.

The EM8504 integrates voltage supervisory functions. Minimum and maximum voltages are controlled on the LTS element to prevent damage to the energy storage element. Harvester minimum voltage monitoring allows stopping the DCDC limiting power loss when no energy can be harvested. Output voltages are kept in a safe range for the application.

To perform granular power management of the application, the EM8504 integrates four independent supply outputs.

It is possible to stop the DCDC converter by setting the pin HRV_DIS to higher than 2.3V.

The EM8504 is available in an industry standard QFN24 4x4 package.

Applications

- Solar energy harvesting equipped platforms
- Wearable systems
- Beacons and wireless sensor networks
- Industrial and environmental monitoring
- Battery operated platforms

Features

- Smart Power Management
  - Ultra-low quiescent current regulator (25nA)
  - 3 auxiliary supplies with high current drive capability
  - Programmable battery output voltage level up to 4.2V
- Ultra-low input voltage and power
  - Cold-start: 0.3V / 3µW
  - Operating: 0.1V / 1µW
- Ultra-low power solution
  - 15 nA in battery protection mode
  - 125 nA when supplying low power applications
- Fast cold-start
  - Fast start-up using dual storage elements
  - Short Term Storage (STS) and Long-Term Storage (LTS)
  - Maintain STS in configurable voltage window when LTS is lower than minimum application voltage
- MPPT
  - Fully embedded Maximum Power Point Tracking (MPPT), optimized for DSSC with fixed Voltage at Maximum Power Point (VMPP)
- Primary Cell Life Time Extension
  - Lifetime of non-rechargeable battery on LTS (harvester assisted)
- Flexible interface
  - SPI or I2C configuration interfaces
- Configuration stored in E2PROM
  - No external passive components required
  - Default configuration values stored in E2PROM
- Power Control
  Extensive configurability of user scenarios:
  - Battery under and over voltage protection
  - Harvesting start/stop (through input pin)
  - STS and LTS voltage status registers
  - Charging start/stop as a function of harvester power
- Temperature range: -40°C to 85°C

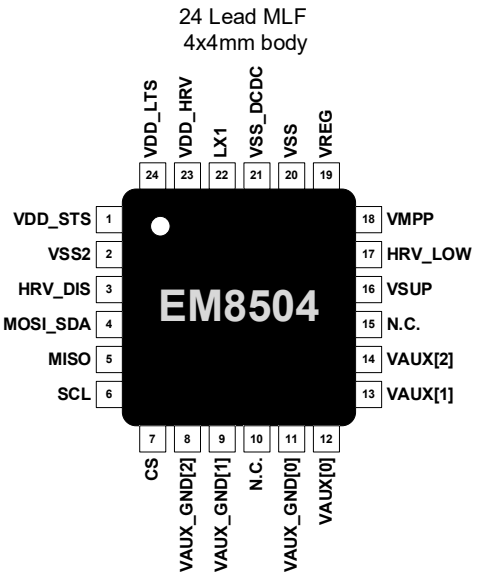

Figure 1-1 QFN24 Package

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ACRONYMS

STS	Short Term Storage. External capacitor of at least 10µF connected to VDD_STS
LTS	Long Term Storage. External rechargeable battery or supercapacitor connected to VDD_LTS
VSUP	Main supply for the application. Regulated with ULP LDO or connected to STS.
VAUX[2:0]	Three optional supplies for additional peripherals. Regulated with VAUX LDO or connected to STS.
HRV	Energy HaRVesting.
DCDC	DC to DC voltage converter transferring energy from the solar cell to STS or LTS.
EFFICIENCY	DCDC efficiency is the ratio between input power, from the solar cell to the output power to LTS (Pout / Pin)
BAT_LOW	Low battery voltage indicator. When at '1', the battery voltage reached the minimum configured level.
HRV_LOW	No solar energy indicator. When at '1', no energy is available from the solar cell.
E²PROM	Non Volatile Memory containing the IC configuration.
CS_DCDC	Cold-start DCDC. Transfers energy from the solar cell to STS at start-up able to operating at 300mV.
MPPT	Maximum Power Point Tracking. Algorithm to extract the maximum power from the solar cell.
VMPP	Voltage point where the solar cell delivers the maximum power.
ULP LDO	Ultra-Low Power LDO to regulates VSUP.
VAUX LDO	3 LDO's regulating respectively VAUX0, VAUX1 and VAUX2
VREG LDO	LDO supplying internal blocks of the EM8504.
VLD	Voltage Level Detector. Constantly check VDD_LTS, VDD_STS and VDD_HRV voltage levels.
SPI	Serial interface on 4 or 3 wires.
I²C	Standard serial interface on 2 wires.
HRV CHECK	Operation during which the EM8504 evaluates the energy level of the solar cell.
T HRV PERIOD	Period between 2 HRV CHECK operations.
T STS PERIOD	Period between 2 STS voltage level measurements
T LTS PERIOD	Period between 2 LTS voltage level measurements

T HRV LOW PERIOD	Period between 2 HRV CHECK operations in HRV_LOW mode.
T LTS HRV LOW PERIOD	Period between 2 LTS voltage level measurements in HRV_LOW mode.

1. PRODUCT DESCRIPTION

The EM8504 is a power management IC with battery charger functions. It manages two energy source elements: a harvester through VDD_HRV, a battery or a Long Term Storage (LTS) through VDD_LTS. The EM8504 provides the supply to the application from these energy sources. Surplus energy is stored in a LTS element.

Features and benefits include:

- **Power management controller, extending application battery life:** the EM8504 supplies the external application through pins VSUP and VAUX[i]. The voltage is delivered directly from VDD_STS or through a regulator. For external devices using an I^2C serial interface, it is possible to disconnect their ground through the use of the auxiliary ground pins (VAUX_GND). This solution avoids supplying the devices connected to a switched-off output supply through the pull-up of I^2C bus. Overall power consumption is reduced by turning off peripheral ICs through the EM8504.

- **Battery charger from harvester source:** EM8504 manages energy harvesting from single/dual junction solar cells. The DCDC boost converter is able to start the application from the harvester source. With its dual storage architecture, application start-up is fast and independent of the battery voltage.

- **Voltage and current supervisor:** The EM8504 includes supervisory functions to detect harvester energy levels (visible through the HRV_LOW pin).
  The EM8504 protects the battery against over voltage conditions and automatically stops charging when a configurable threshold level is reached.

- **Configuration with E^2PROM, no additional external components:** The mode and functional configuration of the EM8504 is controlled by the host MCU through a SPI or an I^2C interface. Voltage supervision thresholds are set by registers. Configuration parameters are held in on-chip non-volatile memory (E^2PROM). The EM8504 default configuration parameter values can be modified by the user.

1.1. OPERATING MODES

The EM8504 operates in two main modes:

1) Normal mode (STS and LTS Connected)
   - V_{LTS} is inside battery operating range.
   - LTS is connected to STS.
   - The system can be configured to disconnect VAUX or/and VAUX_GND pins.

2) LTS protection mode (STS and LTS disconnected)
   - EM8504 enters this mode when V_{LTS} drops below minimum battery operation (v_bat_min_lo).
   - Battery status readable by register in reg_status (see section 5.1).LTS and STS are disconnected to protect LTS against under voltage condition.
   - VSUP and VAUX are maintained through the DCDC converter only.

1.2. VOLTAGE NAMING CONVENTIONS

To describe the operation of this product, the following set of voltage naming conventions is adopted throughout this document , Table 1-1:

NAME	DESCRIPTION
v_bat_max_hi	Maximum battery voltage. High level of hysteresis.
v_bat_min_hi_dis	Minimum STS maintenance voltage – acts as v_bat_min_hi when STS and LTS are disconnected
v_bat_min_hi_con	Minimum battery maintenance voltage – acts as v_bat_min_hi when STS and LTS are connected
v_bat_min_hi	Minimum battery voltage. High level of hysteresis Equal to **v_bat_min_hi_dis** or **v_bat_min_hi_con** according to the connection state in between STS and LTS. The term "**v_bat_min_hi**" is used here whenever there is no specific usage of the connected and disconnected values
v_bat_min_lo	Minimum battery voltage. Low level of hysteresis
v_apl_max_hi	Maximum application voltage. High level of hysteresis
v_apl_max_lo	Maximum application voltage. Low level of hysteresis
V_{cs_hi}	Cold start voltage level
v_ulp_ldo	Regulated voltage on VSUP pin
v_hrv_min	Minimum voltage for switching on/off the DCDC. See §5.2.2 for current or voltage detection selection.

Table 1-1 Voltage Naming Conventions

1.3. BLOCK DIAGRAM

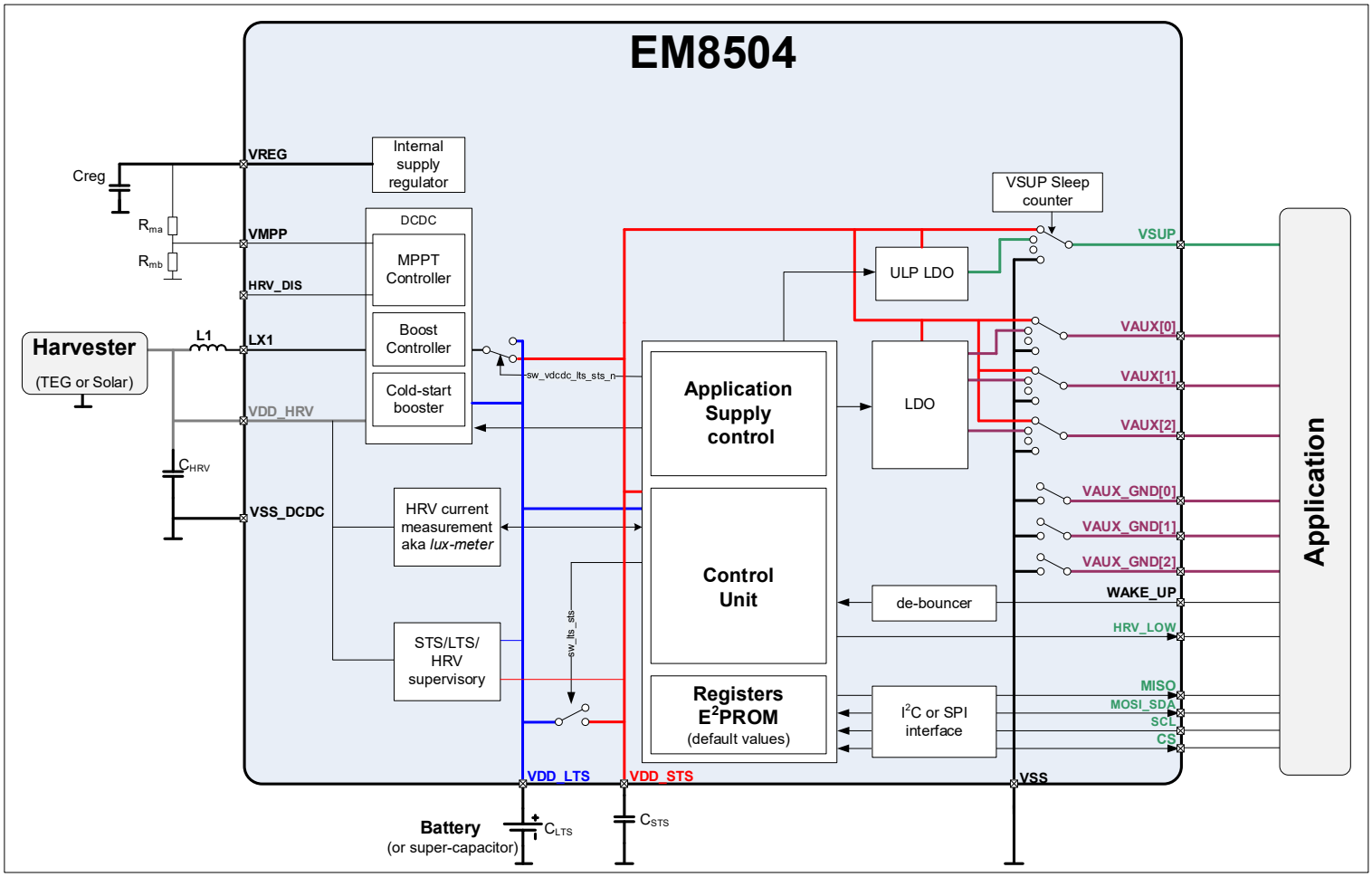


Figure 1-1 EM8504 Block Diagram

1.4. FUNCTIONAL DESCRIPTION

The following paragraphs describe the behavior of VSTS, VLTS and VSUP for a series of typical use cases.

(VAUX supplies have the same behavior as VSUP).

1.4.1. COLD-START ON HARVESTER

This use case outlines a start-up on harvester voltage, with all storage elements discharged or in protection mode.

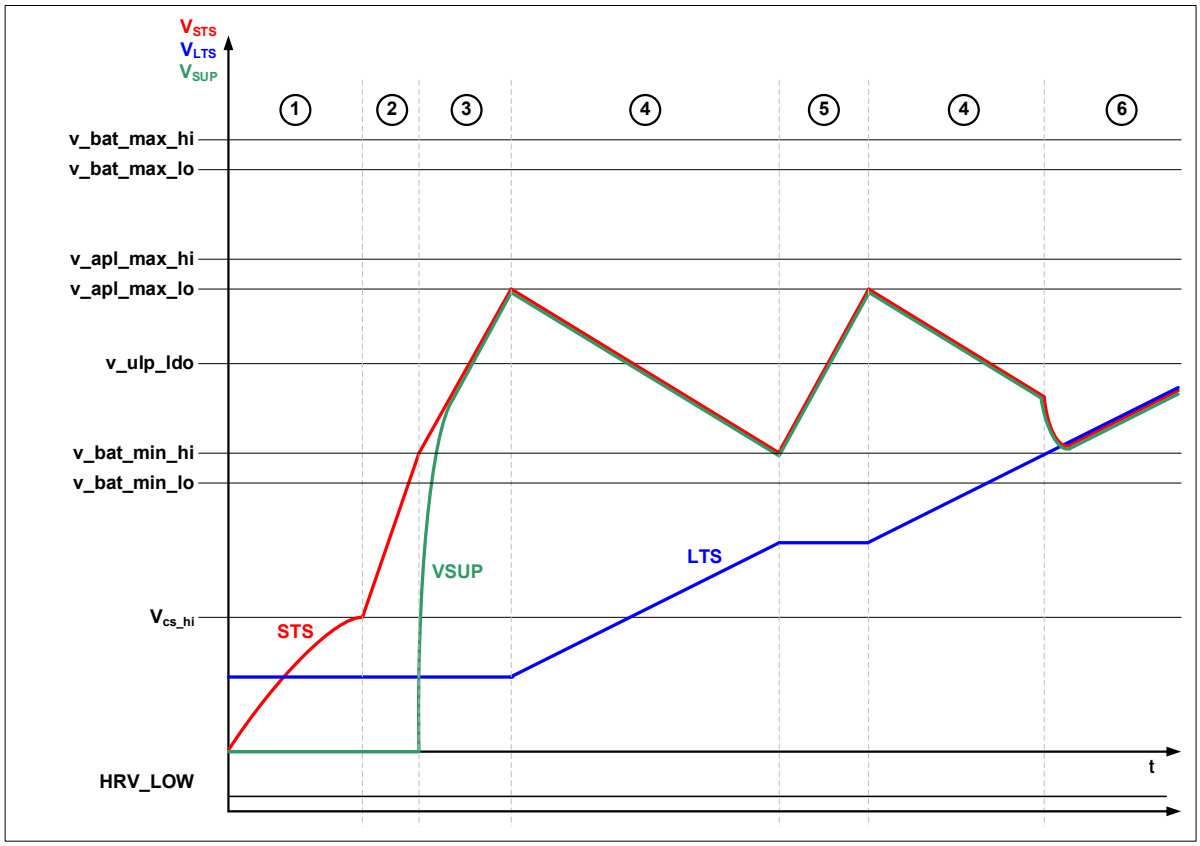


Figure 1-2 Start-up and energy storage sequence when LTS is lower than the cold-start voltage

1. The DCDC starts transferring energy from HRV to STS
2. When V_{STS} is higher than V_{cs_hi}, the cold start sequence ends, the device boots and the DCDC is switched to main charging mode with MPP tracking.
3. When V_{STS} rises above **v_bat_min_hi**, VSUP is connected to STS supplying the application
4. When V_{STS} reaches the maximum application voltage level **v_apl_max_lo**, the DCDC transfers energy into LTS. The application is supplied by the C_{STS} only.
5. When V_{STS} drops to the minimum pre-defined charge value **v_bat_min_hi**, the DCDC transfers energy back into STS
6. The system remains in states 4 & 5 until V_{LTS} is higher than the minimum battery voltage required to supply the external application **v_bat_min_hi**. Then LTS is connected to STS and both storage elements are charged in parallel.

1.4.2. START-UP ON LONG TERM STORAGE (LTS)

This case emulates plugging in a partially charged battery when energy from the harvester is available. The EM8504 starts on LTS voltage, then transfers energy form the harvester to the battery.

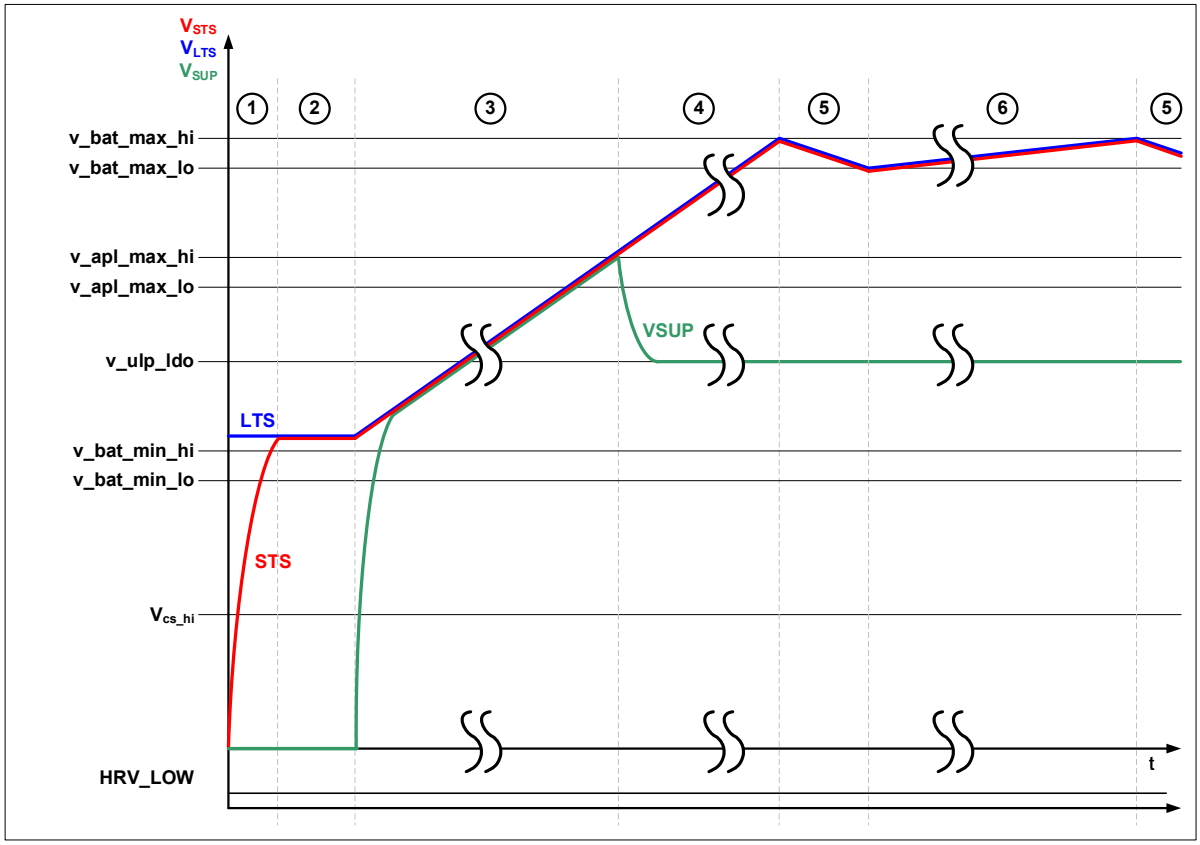


Figure 1-3 Start-up and energy bank sequence when LTS is above the minimum battery level

1. LTS and STS are connected together, V_{STS} quickly reaches V_{LTS}.
2. As V_{STS} reaches $V_{cs\ hi}$, the system boots and then VSUP is connected to STS (which is also connected to LTS).
3. After V_{SUP} reaches V_{LTS} and V_{STS} level, the system reaches the same state as the one described in state 6 of §1.4.1
4. When V_{LTS} (and therefore also V_{STS}) reaches the maximum voltage of the application, VSUP is regulated to **v_ulp_ldo**.
5. When V_{LTS} and V_{STS} reach **v_bat_max_hi** the DCDC stops to protect the battery against over voltage
6. When V_{LTS} and V_{STS} drop to **v_bat_max_lo** the DCDC starts again to charge STS and LTS.
7. The system remains in states 5 & 6 to maintain the battery voltage between **v_bat_max_hi** and **v_bat_max_lo.**

When a battery charged above the maximum application voltage is connected, the system reacts as above except for VSUP, which is regulated from the start due to VSTS/VLTS exceeding the v_apl_max_hi threshold.

1.4.3. SYSTEM SHUT-DOWN

The EM8504 informs the application when the available energy drops below a minimum level required for operation with the register reg_vld_status.lts_bat_min_hi and reg_vld_status.lts_bat_min_lo. After the first warning (reg_vld_status.lts_bat_min_hi = ‘0’ and

reg_vld_status.lts_bat_min_lo = '1'), the device initiates an application shut-down sequence to protect the battery (reg_vld_status.lts_bat_min_hi = reg_vld_status.lts_bat_min_lo = '1').

The first example scenario shows an application drawing more current than the harvester is able to supply. The application is stopped (phase 3). Once re-started, it keeps a low current consumption profile allowing the charging of the LTS energy storage.

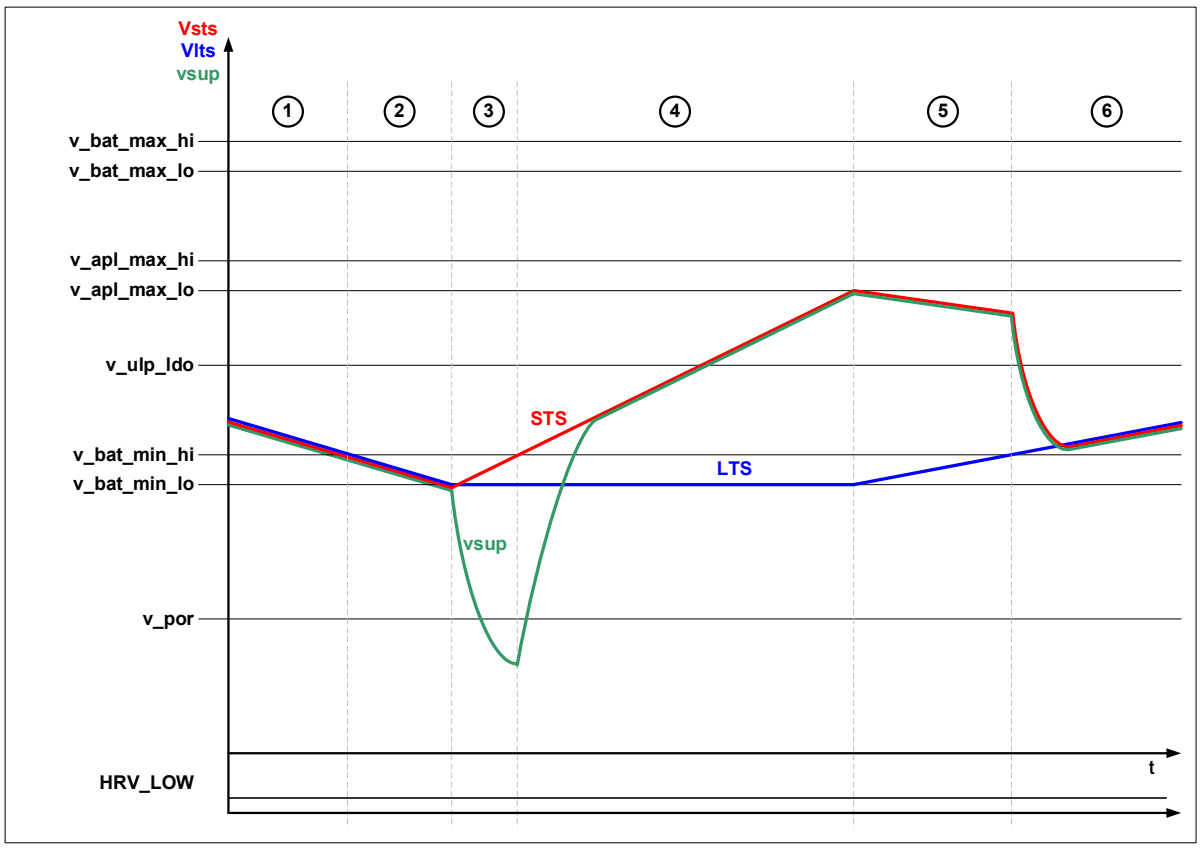


Figure 1-4 Application shut-down with a working harvester

The second example describes the application shut-down sequence when no energy can be harvested from the harvester cell.

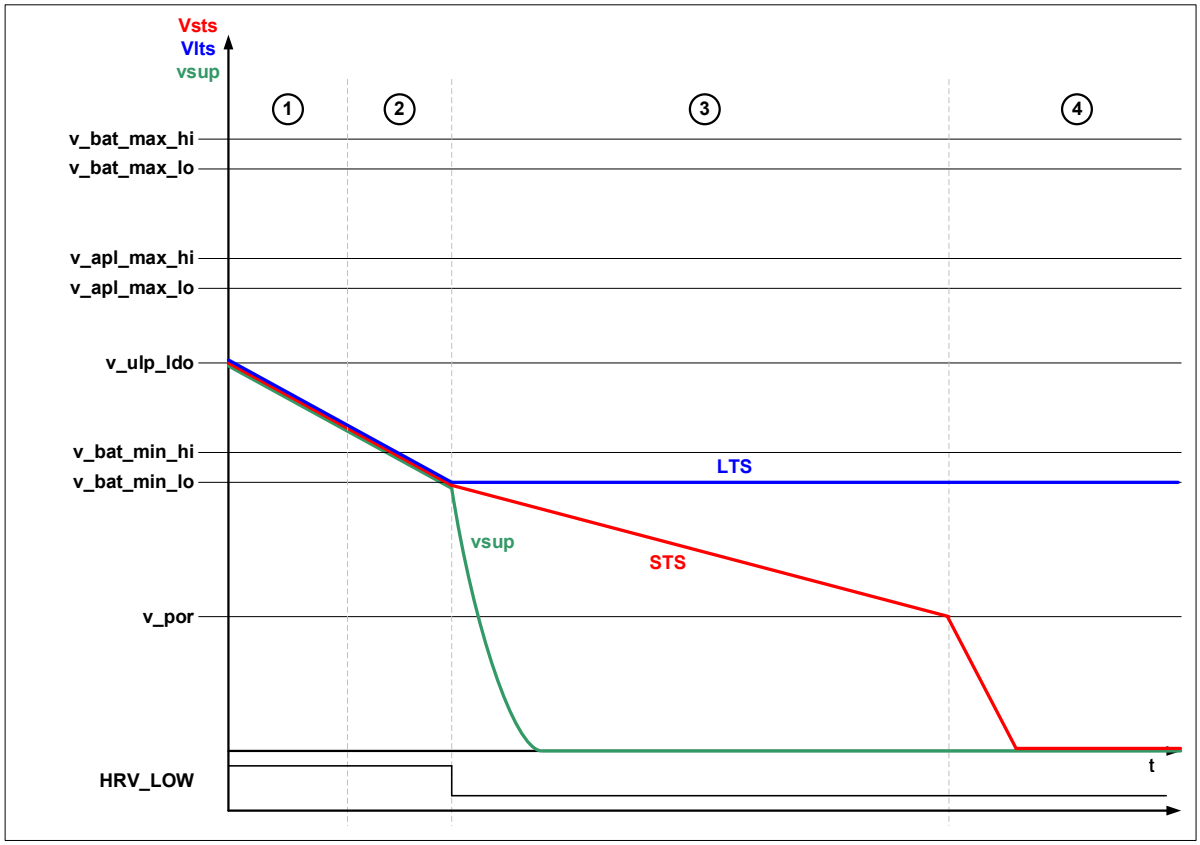


Figure 1-5 Application shut-down without energy from the harvester

2. HANDLING PROCEDURES

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

3. PIN DESCRIPTION

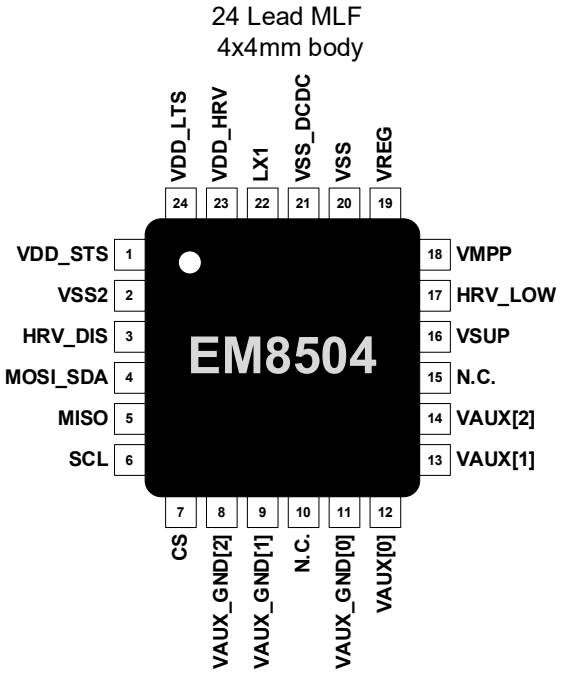


Figure 3-1 QFN24 Package

PIN		I/O TYPE		DESCRIPTION
NO.	NAME	DIRECTION	SUPPLY	
1	VDD_STS	I/O	–	Connection for the Short Term energy Storage element (STS)
2	VSS2	Supply	–	Device ground connection
3	HRV_DIS	Input	–	Stop main DCDC when HRV_DIS > 2.3V
4	MOSI_SDA	Input	VSUP	SPI MOSI or I2C SDA connection
5	MISO	Output	VSUP	SPI MISO connection
6	SCL	Input	VSUP	SPI or I2C clock
7	CS	Input	VSUP	SPI chip select and SPI/I2C selection mode(when at '1')
8	VAUX_GND[2]	Output	–	Auxiliary 2 ground connection
9	VAUX_GND[1]	Output	–	Auxiliary 1 ground connection
10	N.C.			
11	VAUX_GND[0]	Output	–	Auxiliary 0 ground connection
12	VAUX[0]	Output	–	Auxiliary 0 supply output connection
13	VAUX[1]	Output	–	Auxiliary 1 supply output connection
14	VAUX[2]	Output	–	Auxiliary 2 supply output connection
15	N.C.			
16	VSUP	Output	–	Main supply output
17	HRV_LOW	Output	VSUP	Energy harvester cell low indicator (when at '1')
18	VMPP	Input	–	Fixed target voltage
19	VREG	Output	–	Regulated voltage connection
20	VSS	Supply	–	Device ground connection
21	VSS_DCDC	Supply	–	Device ground connection
22	LX1	Input	–	Inductor connection for boost converters
23	VDD_HRV	Input	–	Direct connection from energy harvester
24	VDD_LTS	I/O	–	Connection for the Long Term energy Storage element (LTS)

Table 3-1 Pin-out description

The digital pads are all supplied by VSUP. When VSUP is disabled these pads are floating therefore the communication interface is off. All digital pads are active HIGH.

4. ELECTRICAL SPECIFICATIONS

4.1. ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE MIN	VALUE MAX	UNIT
Power supply VDD_HRV	-0.2	2.0	V
Power supply VDD_STS, VDD_LTS	-0.2	4.6	V
HRV_DIS input voltage range	-0.2	6.0	V
Input voltage	VSS-0.2	V_{SUP}+0.2	V
Input voltage (pin VMPP)	-0.2	2.1	V
Storage Temperature Range (T_{STG})	-65	150	°C
Electrostatic discharge to ANSI/ESDA/JEDEC JS-001-2012 for HBM	-2000	2000	V

Table 4-1 Absolute maximum ratings

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Warning: The device is not functional when exposed to light. When a non-packaged version is used, it is mandatory to protect the device from light (e.g. glob-top, non-transparent package, metal shield on the PCB …)

4.2. OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_{RANGE}	-40	25	85	°C
DC input voltage into VDD_HRV(1)	V_{HRV}	0.1	0.5	1.8	V
Long Term energy Storage bank voltage	V_{LTS}		3.0	4.2	V
Short Term energy Storage bank voltage	V_{STS}		3.0	4.2	V
VMPP voltage	V_{MPP}	0.1	0.5	1.8	V
HRV_DIS voltage	V_{HRV_DIS}		5	5.5	V
Long term capacitor(2)	C_{LTS}	0.001	2		F
Short term capacitor	C_{STS}	10	47		µF
Regulated voltage capacitor	C_{REG}	470			nF
Harvester capacitor (nominal value)	C_{HRV}	4.7		10	µF
VSUP capacitor	C_{SUP}	1		0.1*C_{STS}	µF
VAUX capacitor	C_{AUX}	1		0.1*C_{STS}	µF
Input inductance	L_1	37.6	47	56.4	µH

(1) Cold-start has been completed
(2) When using a super-capacitor

Table 4-2 Operating Conditions

4.3. ELECTRICAL CHARACTERISTICS

Unless otherwise specified: T_A=-40 to +85°C for min max specifications and T_A= 25°C for typical specifications.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
End of cold-start Voltage on VDD_STS	V_{cs_hi}	With V_{STS} increasing		1.3		V
Start of cold-start Voltage on VDD_STS	V_{cs_lo}	With V_{STS} decreasing		1.1		V
Typical DC input voltage range into VDD_HRV		Cold-start completed	0.1		1.8	V
Typical input power range		V_{STS} > V_{cs_hi} V_{VDD_HRV} = 0.5V	0.001		100	mW
Minimum cold-start voltage for charging STS		V_{STS} < V_{cs_lo}		300	1800	mV
Minimum cold-start input power		V_{STS} < V_{cs_lo}		3		µW
Cold-start duration		C_{STS} = 47uF, V_{HRV} = 0.5V, P_{HRV} = 100µW, V_{STS}(0s)=0V, V_{LTS}(0s)=0V, v_bat_min_hi=2V		2		s
CURRENT CONSUMPTIONS ON LTS						
IDD in “LTS protection mode” and “HRV low mode”	I_{LTS_prot1}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled		65		nA
IDD in “LTS protection mode”	I_{LTS_prot2}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled		15		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo2}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled		145		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo3}	Battery supervisory at 4Hz; ULP LDO enabled and VAUX LDO disabled		170		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo4}	Battery supervisory at 4Hz; VSUP and VAUX[0] LDO enabled		285		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo5}	Battery supervisory at 4Hz; VSUP and VAUX[1] LDO enabled		265		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo6}	Battery supervisory at 4Hz; VSUP and VAUX[2] LDO enabled		250		nA
IDD in “HRV low mode” STS and LTS connected	I_{HRV_lo6}	Battery supervisory at 4Hz; VSUP and all VAUX LDO enabled		380		nA
IDD in “normal mode” STS and LTS disconnected	I_{NORM}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled (VDD_STS < VDD_LTS)		45		nA
QUIESCENT CURRENT AND LEAKAGE ON STS (WHEN LTS IS NOT CONNECTED TO STS)						
IDD in “HRV low mode”	I_{STS_hrvlo}	Battery supervisory at 4Hz; VSUP and VAUX LDOs disabled		65		nA
VSUP AND VAUX LDO VOLTAGE LEVEL						
ULP/VAUX LDO level 0		V_{STS} – V_{SUP}> 0.3V	1.08	1.2	1.32	V
ULP/VAUX LDO level 1		V_{STS} – V_{SUP}> 0.3V	1.39	1.55	1.71	V
ULP/VAUX LDO level 2		V_{STS} – V_{SUP}> 0.3V	1.48	1.65	1.82	V
ULP/VAUX LDO level 3		V_{STS} – V_{SUP}> 0.3V	1.62	1.8	1.98	V
ULP/VAUX LDO level 4		V_{STS} – V_{SUP}> 0.3V	1.8	2	2.2	V
ULP/VAUX LDO level 5		V_{STS} – V_{SUP}> 0.3V	1.98	2.2	2.42	V
ULP/VAUX LDO level 6		V_{STS} – V_{SUP}> 0.3V	2.16	2.4	2.64	V
ULP/VAUX LDO level 7		V_{STS} – V_{SUP}> 0.3V	2.34	2.6	2.86	V
VREG LDO (4)						
VREG LDO level	V_{REG_LVL}	V_{STS} > 2.0V	1.38	1.53	1.68	V
VREG maximum external current load	V_{REG_IMAX}	V_{STS} > 2.0V			20	µA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
MAXIMUM CURRENT ON THE ULP AND VAUX LDO						
Maximum current on ULP LDO		Drop from open voltage is 100 mV, LDO level at 1.8V	10			mA
Maximum current on VAUX[0] LDO		Drop from open voltage is 100 mV, LDO level at 1.8V	20			mA
Maximum current on VAUX[1] LDO		Drop from open voltage is 100 mV, LDO level at 1.8V	10			mA
Maximum current on VAUX[2] LDO		Drop from open voltage is 100 mV, LDO level at 1.8V	5			mA
SWITCH RESISTOR						
VDD_LTS to VDD_STS	$R_{sw\_LTS\_STS}$	VDD_STS at 3V		3.1		Ω
VDD_STS to VSUP	R_{sw_VSUP}	VDD_STS at 3V		7.4		Ω
VDD_STS to VAUX[0]	R_{sw_VAUX0}	VDD_STS at 3V		4.4		Ω
VDD_STS to VAUX[1]	R_{sw_VAUX1}	VDD_STS at 3V		5.8		Ω
VDD_STS to VAUX[2]	R_{sw_VAUX2}	VDD_STS at 3V		6.4		Ω
VAUX_GND[0] to VSS	R_{sw_GND0}	VDD_STS at 3V		4.74		Ω
VAUX_GND[1,2] to VSS	$R_{sw\_GND1,2}$	VDD_STS at 3V		5.62		Ω
SUPERVISORY LEVELS ON STS, LTS AND HRV(1)						
Maximum voltage					4.2	V
Level step from lvl0 to lvl15	V_{lvl_15}			73		mV
Level step from lvl16 to lvl30 (1.24V to 2.26V)	V_{lvl_30}		67.9	73	78.1	mV
Level step from lvl31 to lvl54 (2.34V to 4.2V)	V_{lvl_54}		69.4	73	76.7	mV
Differential non linearity				±0.5		LSB
Number of levels				54		
HARVESTER CURRENT LEVEL DETECTOR – LUX METER						
Harvester current level step	$I_{hrv\_check\_lvl}$			1		µA
Luxmeter current detection level "lvl" = level used for the measurement [0..15]	I_{lux_lvl}			2^{lvl}		µA
Short circuit voltage	V_{hrv_scv}			70		mV
DCDC CONTROL						
HRV_DIS threshold level	$V_{ih\_hrv\_dis}$				2.3	V
E2PROM PARAMETERS						
E^2PROM write time	T_{ee_wr}				8	ms
E^2PROM read time	T_{ee_rd}				0.9	ms
E2PROM maximum write cycle	N_{ee_cyc}		1000			
E2PROM read hold time	T_{hd_rd}				10	µs
INTERFACE PARAMETERS						
Input - low level	V_{il_si}	V_{SUP}=1.2V to 3.6V			0.2* V_{SUP}	V
Input - high level	V_{ih_si}	V_{SUP} =1.2V to 3.6V	0.8* V_{SUP}			V
Output – low level for I2C(3)	I_{ol_sda}	V_{SUP} =1.8V, Vol=0.2* V_{SUP}	3			mA
Output – low level for I2C	$I_{ol\_sda\_1.2}$	V_{SUP} =1.20V, Vol=0.23*Vsup	3			mA
Output – low level(3)	I_{ol}	V_{SUP} =1.8V, Vol=0.2*Vsup (MISO, MOSI_SDA, HRV_LOW)	1			mA
Output – low level	$I_{ol\_1.2}$	V_{SUP} =1.20V, Vol=0.23*Vsup (MISO, MOSI_SDA, HRV_LOW)	1			mA
Output – high level(3)	I_{oh}	V_{SUP} =1.8V, Voh=0.8*Vsup (MISO, MOSI_SDA, HRV_LOW)			-1	mA
Output – high level	$I_{oh\_1.2}$	V_{SUP} =1.2V, Voh=0.8*Vsup (MISO, MOSI_SDA, HRV_LOW)			-1	mA
I^2C bus load capacitor	C_b	On MOSI_SDA and SCL			400	pF
SPI TIMINGS						
SPI clock input frequency	F_{spi}				5	MHz
SCL low pulse	T_{low_scl}		20			ns
SCL high pulse	T_{high_scl}		20			ns
MOSI_SDA setup time	T_{setup_mosi}		20			ns
MOSI_SDA hold time	T_{hold_mosi}		20			ns
MISO output delay	T_{delay_miso}	25pF load, V_{SUP} =1.6V min			30	ns
MISO output delay	T_{delay_miso}	25pF load, V_{SUP} =1.2V min			40	ns
CS setup time	T_{setup_cs}		50			ns
CS hold time	T_{hold_cs}		20			ns
I^2C TIMINGS(2)						
MOSI_SDA setup time	t_{sudat}	Standard & Fast Modes	160			ns
		High Speed Mode	30			ns
MOSI_SDA hold time	t_{hddat}	Standard & Fast Modes with C_b =100pF Max.	80			ns
		Standard & Fast Modes with C_b =400pF Max	90			ns
		High Speed Mode with C_b=100pF Max.	18		115	ns
		High Speed Mode with C_b=400pF Max.	24		150	ns
SCL low pulse(3)	t_{low}	High Speed Mode with C_b=100pF Max. V_{SUP} =1.8V	160			ns
SCL low pulse	t_{low}	High Speed Mode with C_b=100pF Max. V_{SUP} =1.2V	210			ns

(1) The **v_bat_min**, **v_bat_max**, **v_apl_min** with their hysteresis can be set according to the supervising levels. E.g. for **v_bat_max**, both **v_bat_max_lo** and **v_bat_max_hi** will have to be set accordingly.
(2) Refers to I^2C specification 2.1 (January 2000)
(3) When reg_ext_cfg.sdi_slope_ctrl = '1'
(4) VREG min/max variation are mainly dominated by process variations not temperature or STS voltage.

Table 4-3 Electrical Specifications

4.4. TIMING DIAGRAMS

4.4.1. SPI INTERFACE

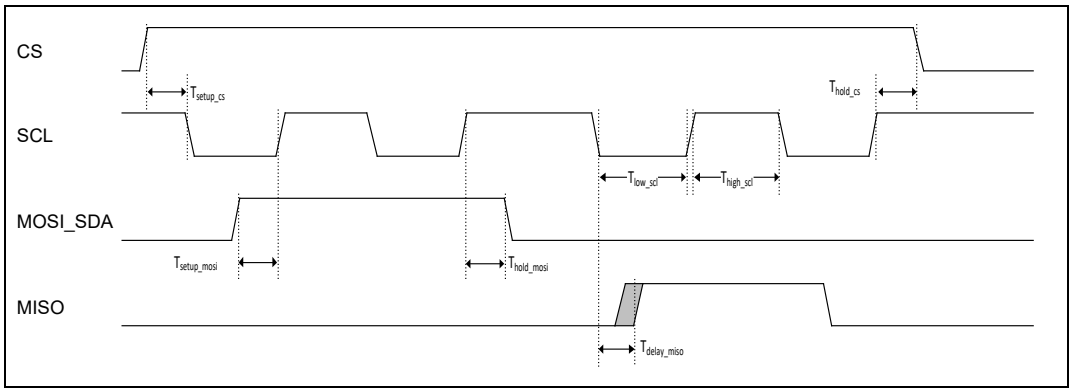


Figure 4-1 4-wire SPI Timing Diagram

4.4.2. I2C INTERFACE

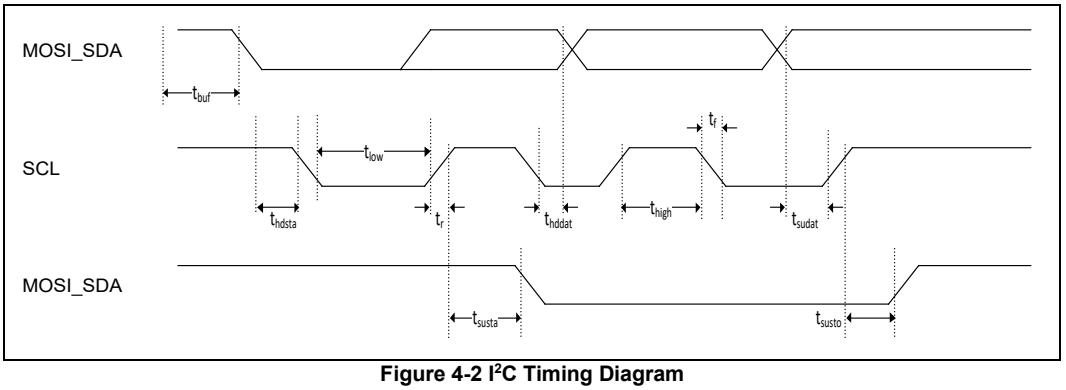


Figure 4-2 I²C Timing Diagram

5. PRODUCT CONFIGURATION

The EM8504 is an autonomous power management system able to manage power domains, power sources and storage elements.

At start-up the device enters a boot sequence. It controls the state of both energy storage elements, and sets the default configuration parameters of the device by retrieving the corresponding values from the on-chip E²PROM.

Upon completion of the boot sequence the system enters the supervising and harvester controller state (“normal mode”). It is now possible to modify configuration parameters through the serial interface to change the behavior of the device. When updating the device configuration through the serial interface it is recommended to write the complete set of EM8504 configuration parameters in a single transaction (see §6).

EM8504 is able to operate autonomously by using default configuration values from the on-chip E²PROM.

5.1. STATUS INFORMATION

EM8504 provides status feed-back as follows.

- To allow fast system response the pin HRV_LOW directly indicates the status of the harvester cell to the host MCU.
- Additional status information is provided through register *reg_status*. During an SPI transaction, the *reg_status* value sent as the first byte (along with the indication from the MCU of the address to be accessed). In case of an I2C transaction the *reg_status* register has to be polled explicitly.

Register Name: reg_status				Address: 0x22
Bits	**Bit name**	**Type**	**Reset**	**Description**
7	eeprom_data_busy	RO	0	• '1' EEPROM being written. Wait for new configuration • '0' EEPROM ready to be written. New configuration can be written
6	hrv_lux_busy	RO	0	• '1' lux-meter or HRV current supervisory is running • '0' no current measurement on the harvester on-going.
5	hrv_low	RO	0	• '1' HRV energy level too low for harvesting • '0' HRV has enough energy to be harvested
4	bat_low	RO	0	• '1' LTS voltage **lower** than **v_bat_min_hi** in normal mode, **lower** than **v_bat_min_lo** in primary cell mode • '0' LTS voltage **higher** than **v_bat_min_hi** in normal mode, **higher** than **v_bat_min_lo** in primary cell mode
3	sw_vdcdc_lts_nsts	RO	0	• '1' DCDC is charging LTS • '0' DCDC is charging STS
2	sw_lts_sts	RO	0	• '1' LTS and STS are connected • '0' STS is disconnected from LTS
1	hrv_dis	RO	0	• '1' HRV_DIS detected • '0' DCDC is running if HRV energy available and battery not fully charged
0	lts_protect	RO	0	• '1' LTS protection mode activated (V_{LTS} < **v_bat_min_lo**) • '0' LTS protection mode inactive (V_{LTS} > **v_bat_min_lo**)

Table 5-1 Status Register (0x22)

EM8504 offers great flexibility in being configured for different system applications and use cases. The following chapters provide detailed descriptions of all configuration parameters and registers available to the user.

5.2. SUPERVISING AND HARVESTER CONTROLLER BEHAVIOUR

5.2.1. STORAGE ELEMENT

Storage element voltage and state are available through the *reg_vld_status* register.

Register name: reg_vld_status				Address: 0x23
Bits	**Bit name**	**Type**	**Reset**	**Description**
7	lts_bat_min_hi	RO	0	• '1' V_{LTS} > **v_bat_min_hi** • '0' V_{LTS} <= **v_bat_min_hi**
6	lts_bat_min_lo	RO	0	• '1' V_{LTS} > **v_bat_min_lo** • '0' V_{LTS} <= **v_bat_min_lo**
5	sts_bat_max_hi	RO	0	• '1' V_{STS} > **v_bat_max_hi** • '0' V_{STS} <= **v_bat_max_hi**
4	sts_bat_max_lo	RO	0	• '1' V_{STS} > **v_bat_max_lo** • '0' V_{STS} <= **v_bat_max_lo**
3	sts_apl_max_hi	RO	0	• '1' V_{STS} > **v_apl_max_hi** • '0' V_{STS} <= **v_apl_max_hi**
2	sts_apl_max_lo	RO	0	• '1' V_{STS} > **v_apl_max_lo** • '0' V_{STS} <= **v_apl_max_lo**
1	sts_bat_min_hi	RO	0	• '1' V_{STS} > **v_bat_min_hi** • '0' V_{STS} <= **v_bat_min_hi**
0	sts_bat_min_lo	RO	0	• '1' V_{STS} > **v_bat_min_lo** • '0' V_{STS} <= **v_bat_min_lo**

Table 5-2 Voltage Status Register (0x23)

Operation of the two energy banks (LTS and STS) is performed through three key voltage threshold levels.

- Minimum battery level voltage **v_bat_min** (reg_v_bat_min_hi_con or *reg_v_bat_min_hi_dis* and *reg_v_bat_min_lo*)
- Maximum battery level voltage **v_bat_max** (*reg_v_bat_max_hi* and *reg_v_bat_max_lo*)
- Maximum application level voltage **v_apl_max** (*reg_ v_apl_max_hi* and *reg_v_apl_max_lo*)

The three levels include hysteresis settings to avoid instability of the controller. The hysteresis values have to be carefully chosen according to the application and have to fulfill the following conditions:

- v_bat_min_hi_dis > v_bat_min_hi_con > v_bat_min_lo
- v_apl_max_hi > v_apl_max_lo
- v_bat_max_hi > v_bat_max_lo

If v_apl_max ≥ v_bat_max the application maximum level is considered to be the maximum battery level.

Supervision of the minimum battery level is performed through two registers for its highest control level (v_bat_min_hi). When the two battery banks are not connected **v_bat_min_hi_dis** is used to inform the system when it has to charge STS again (see phase 4 to 5 in Figure 1-2 on page 8). When LTS and STS are connected together **v_bat_min_hi_con** is used as supervising level.

The minimum value allowed for the **v_bat_min_hi_dis** register is 0x15 corresponding to typically 1.47 V. For any value lower than this minimum the system may shut-down without notification through reg_vld_status.lts_bat_min_hi.

All voltage levels with prefix "*v_*" are configured by register according to the following equation:

$$v\_\langle voltage\ name\rangle = V_{lvl} * (reg\_\langle voltage\ name\rangle + 1)$$

The EM8504 protects the battery when its voltage is too low. This corresponding threshold level can be set through the **v_bat_min_lo** register. When V_{LTS} is falling below this value the EM8504 disconnects and protects LTS element.

5.2.2. HARVESTER POWER SUPERVISORY FUNCTIONS

The EM8504 monitors harvester power to disable DCDC operation when no energy is available.

The mechanism for harvester monitoring uses the same Voltage Level Detector used for the supervision of LTS and STS. It checks that VHRV > detection level defines by the register reg_v_hrv_min(5:0) as depicted in Table 5-3.

Register name: reg_v_hrv_cfg			Address: 0x04	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7	–	–	Reserved	
6	hrv_check_vld	RW	Must be set to '1'	
5:0	v_hrv_min	RW	Minimum HRV open voltage required to generate energy. $V_{hrv\_min} = V_{lvl} * (reg\_v\_hrv\_min(5:0)+1)$ if $V_{HRV} < V_{hrv\_min}$ and *reg_v_hrv_cfg.hrv_check_vld* = '1' then *reg_status.hrv_low* = '1'	

Table 5-3 Minimum HRV voltage (0x04)

When LTS and STS are not connected internally (in "primary cell mode" or in "battery protection mode") the DCDC booster is able to deliver up to around 1mW maximum to the application. This value depends on input (VDD_HRV) and output (VDD_STS) voltages.

5.2.3. TIMING CONFIGURATION

In addition to voltage level supervision, the user can select independent values for the frequency of supervision on LTS, STS and the harvester. The frequency influences the overall EM8504 power consumption and therefore its efficiency.

The STS and LTS measurement periods are set through the registers *reg_t_sts_period* and *reg_t_lts_period*. The system stops the DCDC pumping process for a short time with a period of t_hrv_period (see Figure 5-1 & Table 5-4) to reset the harvesting controller. The duration of the DCDC disable period is fix and about 125µs.

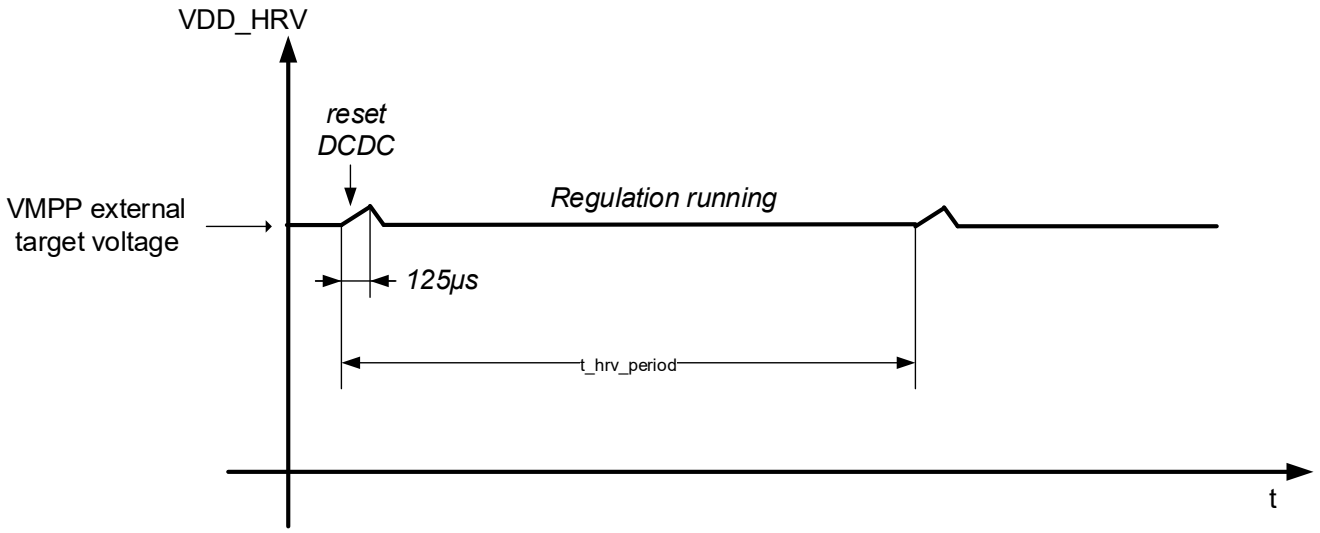


Figure 5-1 DCDC Regulation Timings

Register value	t_hrv_period	t_sts_period	t_lts_period	t_hrv_low_period	t_lts_hrv_low_period
0x00	256 ms	1 ms	1 ms	256 ms	2 ms
0x01	512 ms	2 ms	4 ms	512 ms	8 ms
0x02	1 s	8 ms	16 ms	1 s	32 ms
0x03	2 s	16 ms	64 ms	2 s	128 ms
0x04	4 s	32 ms	256 ms	4 s	512 ms
0x05	8 s	64 ms	1 s	8 s	2 s
0x06	16 s	128 ms	4 s	16 s	8 s
0x07	32 s	256 ms	16 s	32 s	32 s

Table 5-4 Timing Configuration

When entering in “HRV low mode”, monitoring of LTS and the harvester remains active, however the monitoring frequency can be adapted to a situation where the system cannot take energy anymore from the harvester source. The measurement period is then set in parameter **t_hrv_low_period.** In this mode STS is not fed by the harvester anymore. If STS and LTS are not connected internally, STS will collapse. No monitoring is performed on STS.

When the harvester is monitored (*reg_v_hrv_cfg.hrv_check_vld)* based on the voltage measurement, the sampling value is set at the same frequency as the harvester voltage check. However, if the current level detector is used, the measurement of the current is done alternatively with the MPP target setting, dividing the effective frequency of measurement by 2. For example if T_{hrv_period} is set to 4 s, the period for checking the harvester voltage is 8 s, as well as the one for the MPP target setting, and the harvester current checking is done 4 s after the MPP target setting.

5.2.4. MAXIMUM POWER POINT TRACKING

To efficiently support different DC sources, EM8504 offers a configurable MPPT controller with external resistors. The MPP target voltage applied on VMPP indicates to the DCDC what level it has to regulate on VDD_HRV. This target voltage must be set at the point the solar cell delivers the maximum power.

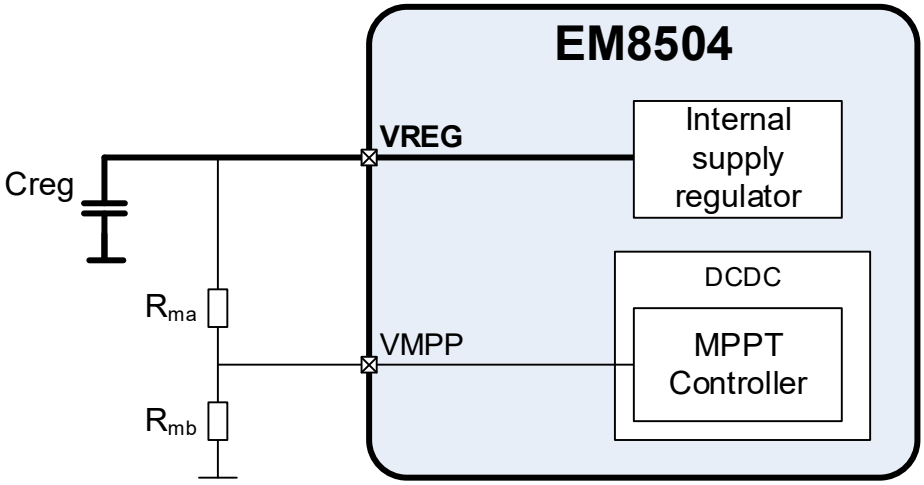


Figure 5-2 MPP configuration block diagram

Rma and Rmb should be calculated so that the load current on VREG never exceeds V_{REG_IMAX} (see Table 4-3).

1. Calculate Rmb:

$$R_{MB} = \frac{V_{MPP}}{I_{REG}}$$

2. Calculate Rma:

$$R_{MA} = \frac{V_{REG}}{I_{REG}} - R_{MB}$$

5.3. POWER MANAGEMENT FUNCTIONS

The EM8504 controls four independent power supply outputs.

The VSUP power supply output is connected to STS when STS level is within the application voltage range ([**v_bat_min**:**v_apl_max**]) or to an LDO (when above **v_apl_max**) to regulate the output to a given value.

The three auxiliary supply outputs VAUX [0:2], are user configurable between STS and the internal LDO. It is possible to force the use of the LDO even though the STS voltage level is compatible with the application supply requirements.

During the boot phase – which corresponds to the set-up of the device – all the power supply outputs are floating. Once the set-up of the registers is completed the supply output values are determined by configuration registers *reg_ldo_cfg.vsup_tied_low* and *reg_vaux_cfg.vaux[x]_cfg*.

The main application power supply (VSUP) is intended to be connected to the application controller. When connected to the LDO its maximum power is limited as LDO is optimized for low consumption. The VSUP supply output is controlled by the *reg_ldo_cfg* register. The value of the LDO is configurable through *reg_ldo_cfg.v_ulp_ldo*. The LDO enable can be forced with *reg_ldo_cfg.frc_ulp_ldo*. When disabled, VSUP can be grounded (*reg_ldo_cfg.vsup_tied_low* = '1') or floating (*reg_ldo_cfg.vsup_tied_low* = '0') (see §5.4).

The individual configurability of the three auxiliary supply outputs allows the creation of different power domains for the external application. The auxiliary outputs are split into the supply and ground pins where all six outputs can be switched on/off independently. The behavior of the VAUX pins is controlled through the *reg_vaux_cfg* register. *reg_vaux_cfg*.v_aux_*ldo* controls the level of the single LDO connected to the three auxiliary supplies.

When switched on (*reg_pwr_mgt.vaux[i]_en* = '1') the auxiliary supply output is controlled by *reg_vaux_cfg.vaux[i]_cfg*.

Four possible settings are available to the user:

1) Force the connection to STS
2) Force the connection to the LDO
3) Use the automatic configuration permitting the auxiliary output to float when STS drops below **v_bat_min**
4) Use the automatic configuration grounding the auxiliary output when STS drops below **v_bat_min**

The automatic configuration of the auxiliary supplies ensures that the auxiliary output voltage is kept within the application voltage range by auto-connecting the supply output to the LDO when STS voltage is exceeding the **v_apl_max** value.

When the power supply output is switched off (*reg_pwr_mgt.vaux[i]_en* = '0'), its configuration is also controlled by the *reg_pwr_mgt.vaux[i]_cfg* register. The output is grounded if *reg_pwr_mgt.vaux[i]_cfg* is set to 3 (b11), otherwise it is kept floating.

When the LDO is used on VSUP or VAUX pins, changing the LDO settings does not generate over or under shoots on the output power supply terminals.

EM8504 offers the possibility to control the ground pin as part of the application, by connecting it to the ground of the EM8504 or letting it float. It is of particular interest when involving applications that are using I^2C communication through the pulls of the I^2C lines. The configuration of the VAUX_GND pins is controlled through the *reg_pwr_mgt.vaux_gnd[i] en* register.

Register name: reg_ldo_cfg			Address: 0x0E	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7	vsup_tied_low	RW	When set to '1', connects VSUP pin to ground when VSUP is disabled, otherwise VSUP remains floating.	
6:4	v_vaux_ldo	RW	VAUX LDO regulated voltage selection • "000" (0) 1.2 V • "001" (1) 1.55 V • "010" (2) 1.65 V • "011" (3) 1.8 V • "100" (4) 2.0 V • "101" (5) 2.2 V • "110" (6) 2.4 V • "111" (7) 2.6 V	
3	frc_ulp_ldo	RW	Force ULP LDO on as soon as V_{STS} > **v_bat_min_hi**	
2:0	v_ulp_ldo	RW	ULP LDO regulated voltage selection • "000" (0) 1.2 V • "001" (1) 1.55 V • "010" (2) 1.65 V • "011" (3) 1.8 V • "100" (4) 2.0 V • "101" (5) 2.2 V • "110" (6) 2.4 V • "111" (7) 2.6 V	

Table 5-5 VSUP output supply and LDOs configuration register (0x0E)

Register name: reg_pwr_cfg			Address: 0x0F	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
5	-	-	Reserved	
6	dis_vaux_gnd2_hrv_low	RW	• '1' open the VAUX_GND[2] (pin is floating) in "HRV low" mode. • '0' Keep the same behavior as in normal mode	
5	dis_vaux_gnd1_hrv_low	RW	"HRV low" mode VAUX_GND[1] behavior. same as for pin VAUX_GND[2]	
4	dis_vaux_gnd0_hrv_low	RW	"HRV low" mode VAUX_GND[0] behavior. same as for pin VAUX_GND[2]	
3	dis_vaux2_hrv_low	RW	• '1' Disable vaux[2] in "HRV low" mode. It is configured by *reg_vaux_cfg.vaux2_cfg* • '0' Keeps its normal mode configuration.	
2	dis_vaux1_hrv_low	RW	"HRV low" mode VAUX[1] behavior. same as for pin VAUX[2]	
1	dis_vaux0_hrv_low	RW	"HRV low" mode VAUX[0] behavior. same as for pin VAUX[2]	
0	dis_vsup_hrv_low	RW	• '1' Disable VSUP in "HRV low" mode. Its behavior is defined by *reg_ldo_cfg.vsup_tied_low* • '0' Keeps its normal mode configuration	

Table 5-6 "HRV low" mode power switch configuration register (0x0F)

Register name: reg_vaux_cfg			Address: 0x10	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7:6	–	–	Reserved	
5:4	vaux2_cfg	RW	Configuration of VAUX[2] pin • "00" (0) Constantly connected to STS • "01" (1) Constantly connected to the LDO • "10" (2) Automatic configuration – floating when below V_{STS} < **v_bat_min** • "11" (3) Automatic configuration – grounded when below V_{STS} < **v_bat_min** If VAUX[2] is disconnected – VAUX[2] is connected to ground if the value is "11", otherwise it is floating	
3:2	vaux1_cfg	RW	Configuration of VAUX[1] pin – same as for VAUX[2] pin	
1:0	vaux0_cfg	RW	Configuration of VAUX[0] pin – same as for VAUX[2] pin	

Table 5-7 Auxiliary supply configuration register (0x10)

Register name: reg_vaux_gnd_cfg			Address: 0x11	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7:3	–	–	Reserved	
2	vaux_gnd2_cfg	RW	• '1' Auto disconnect when V_{STS} not within [**v_bat_min**.. **v_apl_max]** • '0' Fully manual connection	
1	vaux_gnd1_cfg	RW	Configuration of VAUX_GND[1] pin – same as for VAUX_GND [2] pin	
0	vaux_gnd0_cfg	RW	Configuration of VAUX_GND[0] pin – same as for VAUX_GND[2] pin	

Table 5-8 Auxiliary ground pins configuration register (0x11)

Register name: reg_pwr_mgt			Address: 0x19	Value at start-up mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7	frc_prim_dcdc_dis	RW	• '1' Force the DCDC off • '0' Keep the automatic mode of the DCDC	
6	vaux_gnd2_en	RW	Enable the VAUX_GND[2] connection (see *reg_vaux_gnd_cfg.vaux_gnd2_cfg*) when V_{STS} > **v_bat_min_hi**	
5	vaux_gnd1_en	RW	Enable the VAUX_GND[1] connection (see *reg_vaux_gnd_cfg.vaux_gnd0_cfg*) when V_{STS} > **v_bat_min_hi**	
4	vaux_gnd0_en	RW	Enable the VAUX_GND[0] connection (see *reg_vaux_gnd_cfg.vaux_gnd0_cfg*) when V_{STS} > **v_bat_min_hi**	
3	vaux2_en	RW	Enable the VAUX[2] connection (see *reg_vauxcfg.vaux2_cfg*) when V_{STS} > **v_bat_min_hi**	
2	vaux1_en	RW	Enable the VAUX[1] connection (see *reg_vauxcfg.vaux1_cfg*) when V_{STS} > **v_bat_min_hi**	
1	vaux0_en	RW	Enable the VAUX[0] connection (see *reg_vauxcfg.vaux0_cfg*) when V_{STS} > **v_bat_min_hi**	
0	–	–	Reserved	

Table 5-9 Power switch enable register (0x19)

5.4. PRIMARY CELL CONFIGURATION

The EM8504 supports supplying an application through a combination of a primary cell and a harvesting element by setting *reg_lts_cfg.prim_cell* to '1'.

In this case the application is mainly supplied by STS. LTS is automatically connected to STS as soon as the harvesting element is not providing enough energy to supply the application. LTS is disconnected from STS as soon as the harvester provides enough energy to the system again.

LTS and STS are connected automatically when HRV_LOW is asserted, or if after a measurement of V_{STS} below **v_bat_min_hi_dis**, a successive measurement (1 ms later) on STS confirms that the level is still below **v_bat_min_hi_dis**. The connection remains for two periods of HRV measurements.

If the battery level is below **v_bat_min_lo**, STS and LTS are kept disconnected to avoid damaging the battery cell.

The checks on the harvester and STS are done with the same frequencies as shown in §5.2.1.

It is possible to force the connection between STS and LTS, preventing the use of the DCDC converter to harvest energy from the harvester cell – *reg_lts_cfg.prim_cell_connect* = '1'. This is particularly useful to perform high energy tasks.

When the device is in LTS protect mode (*reg.status.lts_protect = '1'*) forcing the primary cell connection has no effect. The system continues to be supplied by the harvester. Forcing a connection leads to the collapse of the supply as the battery is too low.

By permanently connecting STS and LTS it is also possible to use only a primary cell (without harvester) and taking advantage of the EM8504 power management features to control the 4 power supply domains and their automated modes.

Register name: reg_lts_cfg			Address: 0x06	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7:3	–	–	Reserved	
2	prim_cell_connect	RW	• '1' Connect LTS and STS if reg_lts_cfg.prim_cell = '1'. • '0' Normal mode on STS	
1	prim_cell	RW	• '1' Sets the device in primary cell mode. The DCDC never charges LTS • '0' Sets the device in secondary cell mode (LTS is rechargeable)	
0	no_bat_protect	RW	• '1' Disables the battery protection feature. (reg.status.lts_protect = '0') • '0' Enables the battery protection feature.	

Table 5-10 LTS configuration register (0x06)

When the primary cell mode is selected the lux-meter function can only be used when both LTS and STS are forced to be connected together – *reg_lts_cfg.prim_cell_connect* = '1'.

5.5. LUX-METER

The device contains this specific element to determine ranges of current supplied by the harvesting element.

The lux-meter is able to run in three modes:

- Fully automatic mode
- Automatic range selection
- Fully manual mode

In fully automatic mode (selected by writing '1' in *reg_lux_meter_cfg.lux_meter_auto_meas*) the device determines the value range for the current flowing in from the harvesting element. The result is available in the reg_lux_meter_result.lux_meter_result register field. The *reg_lux_meter_result.lux_meter_busy* bit indicates that the measurement is still ongoing and that the result is not available yet.

In automatic range selection mode (selected by writing '1' in *reg_lux_meter_cfg.lux_meter_auto_rng)* the EM8504 automatically determines the optimal range, and measures the voltage at VDD_HRV for maximum precision. The *reg_lux_meter_result.lux_meter_busy* bit indicates that the range search is complete. In this mode lux-meter continues to operate until user disabled by writing '0' into the *reg_lux_meter_cfg.lux_meter_auto_rng*.

The full manual mode allows the user to select the range. The mode is selected by writing on the bit *reg_lux_meter_cfg.lux_meter_manu* – '1' to activate the mode, and '0' to deactivate it. The selection of the range is done through the *reg_lux_meter_cfg.lux_lvl* field.

In case a lux-meter action is requested with LTS and STS disconnected, V_{LTS} < **v_bat_min_lo** or – in primary cell mode – when *reg_lts_cfg.prim_cell_connect* = '0' the action is disregarded and the result – in automatic mode – is invalid.

Register name: reg_lux_meter_cfg				Address: 0x1C
Bits	**Bit name**	**Type**	**Reset**	**Description**
7	–	–	0	Reserved
6	lux_auto_meas	OS	0	Start the automatic lux-meter measurement. The lux-meter is disabled automatically when the measure is finished
5	lux_auto_rng	RW	0	Enable the lux-meter, and search for the best range. It remains enabled
4	lux_manu	RW	0	Enable the lux-meter in manual mode (range forced by *reg_lux_meter_cfg.lux_lvl*)
3:0	lux_lvl	RW	0x0	Target current level to be detected • "0000" (0x0) 1 µA • "0001" (0x1) 2 µA • "0010" (0x2) 4 µA • "0011" (0x3) 8 µA • "0100" (0x4) 15 µA • "0101" (0x5) 30 µA • "0110" (0x6) 60 µA • "0111" (0x7) 120 µA • "1000" (0x8) 0.25 mA • "1001" (0x9) 0.5 mA • "1010" (0xA) 1 mA • "1011" (0xB) 1.8 mA • "1100" (0xC) 3.2 mA • "1101" (0xD) 6 mA • "1110" (0xE) 11 mA • "1111" (0xF) 17 mA

Table 5-11 Lux Meter Configuration Register (0x1C)

Register name: reg_lux_meter_result				Address: 0x1D
Bits	**Bit name**	**Type**	**Reset**	**Description**
7:5	–	–	'000'	Reserved
4	lux_meter_busy	RO	0	Indicates that the lux-meter is still searching for best range
3:0	lux_meter_result	RO	0x0	Lux-meter range status (result in automatic measurement mode) • "0000" (0x0) below 2 µA • "0001" (0x1) from 2 µA to 4 µA • "0010" (0x2) from 4 µA to 8 µA • "0011" (0x3) from 8 µA to 15 µA • "0100" (0x4) from 15 µA to 30 µA • "0101" (0x5) from 30 µA to 60 µA • "0110" (0x6) from 60 µA to 120 µA • "0111" (0x7) from 120 µA to 0.25 mA • "1000" (0x8) from 0.25 mA to 0.5 mA • "1001" (0x9) from 0.5 mA to 1 mA • "1010" (0xA) from 1 mA to 1.8 mA • "1011" (0xB) from 1.8 mA to 3.2 mA • "1100" (0xC) from 3.2 mA to 6 mA • "1101" (0xD) from 6 mA to 11 mA • "1110" (0xE) from 11 mA to 17 mA • "1111" (0xF) above 17 mA

Table 5-12 Lux-meter Result Register (0x1D)

5.6. MISCELLANEOUS FUNCTIONS

This chapter describes additional control functions related to the regulation loop.

5.6.1. SOFT RESET FUNCTION

The soft reset function restarts the EM8504 from its boot sequence. The behavior of the EM8504 is the same as in a normal boot sequence. A soft reset is generated by setting the register *reg_soft_res_word* to 0xAB. This register is enabled only if *reg_protect_key* is set to 0xE2. If the value of the *reg_protect_key* is different from 0xE2, the register *reg_soft_res_word* is set to 0x00.

The *reg_protect_key* register is reset by the soft reset. Creating a new soft sequence requires preloading the *reg_protect_key* again.

Register name: reg_soft_res_word				Address: 0x1A
Bits	**Bit name**	**Type**	**Reset**	**Description**
7:0	soft_res_word	RW	0x00	Force reset when set at 0xAB

Table 5-13 Soft reset register (0x1A)

Register name: reg_protect_key				Address: 0x1B
Bits	**Bit name**	**Type**	**Reset**	**Description**
7:0	protect_key	RW	0x00	Allow writing on *reg_soft_res_word* register when set at 0xE2 Allow writing on protected registers when set at 0x4B Allow writing on E2PROM when set at 0xA5

Table 5-14 Protected registers key (0x1B)

5.6.2. REGISTER PROTECTION

The EM8504 functionality is determined by the content of the configuration registers (like the supervising levels or periods). The registers are always accessible in read mode. Some registers are write protected against unwanted write operations.

The registers in address space range 0x00 to 0x18 are write protected. Writing into these registers is enabled after setting *reg_protect_key* to 0x4B.

Note: The *reg_protect_key* is reset at the end of the communication transaction (see §6 on page 24). It is necessary to set it on the same communication transaction – on SPI keeping CS to '1' or on I^2C before putting a I^2C stop.

Write access to the on-chip E^2PROM is controlled by the same mechanism. Prior to a write operation into the E^2PROM *reg_protect_key* must be set to 0xA5.

5.6.3. LTS PROTECTION DISABLE

By default the EM8504 monitors the battery minimum voltage limit to prevent damage to the LTS energy storage element.

This protection can be disabled by setting register *reg_lts_cfg.no_bat_protect* leaving the system connected to LTS even when the voltage level drops below **v_bat_min**. Disabling protection might be suitable for systems using super-caps or solid-state battery storage elements.

When LTS protection is active the EM8504 tries to start-up from LTS only once, if after booting it still detects that V_{LTS} < **v_bat_min** it enables the protection and never tries to restart from LTS. The system will then re-start as from a standard cold-start.

5.6.4. DCDC OFF FORCING

There are two ways to force off the DCDC:

5.6.4.1. SOFT MODE

It is possible to stop the regulation loop by explicitly forcing the DCDC to stop its pumping operation. To stop the DCDC it is necessary to set the bit *reg_pwr_mgt.frc_prim_dcdc_dis* to '1' (see Table 5-9). De-asserting this bit (write it to '0') will re-enable the DCDC to its normal operation. If STS drops below v_bat_min_lo, the system will automatically restart the DCDC even if the register *reg_pwr_mgt.frc_prim_dcdc_dis*is at '1'.

5.6.4.2. HARD MODE

The input pin HRV_DIS allows stopping the DCDC harvesting. When HRV_DIS > $V_{ih\_hrv\_dis}$ (see Table 4-3), the DCDC stops transferring energy from the Solar cell to storage elements. This feature has priority over the status of STS and LTS. Nothing prevent STS from dropping below V_{cs_lo}. In that case, the EM8504 enters power on reset mode and the cold-start DCDC will turn on and transfer energy from the solar cell into STS even if HRV_DIS is at '1'.

6. SERIAL INTERFACE

The EM8504 offers SPI and I²C serial interfaces selected by the CS pin.(see §6.2.1).

The configuration/function of the EM8504 is updated only after the end of a communication transaction. An SPI transaction is defined by all the bytes sent and received when the pad CS is kept to '1'. An I²C transaction is defined by all the data sent or received between a start and a stop I²C patterns.

Data synchronization between the communication interface and the internal part of the device is done at the end of a supervising loop. New information is active two milliseconds after the end of the transaction. All write transactions sent before the end of this synchronization interval are ignored. It is recommended to perform the device configuration in one transaction. Read transactions are allowed at any time.

6.1. I2C INTERFACE

The I²C slave interface is compatible with Philips I²C Specification version 2.1 (see specific timings on electrical specifications chapter). All modes (standard, fast, high speed) are supported. MOSI_SDA and SCL pins are not strictly open-drain (they include protection diodes to VSUP).

The 7-bit device address is defined in the E²PROM (at address 0x58). This address is copied at boot into the *reg_spi_i2c_cfg.ic2_addr* register field.

The I²C bus uses the 2 wires SCL (Serial Clock) and MOSI_SDA. CS has to be connected to VSS. MOSI_SDA is bi-directional with open drain to VSS: it must be externally connected to VSUP via a pull up resistor.

The I2C interface supports single and multiple read and write transactions.

In the following figures, "S" indicates the I²C transaction start, "P" indicates the I²C transaction stop.

The multi-read and multi write transactions are described in the following figures.

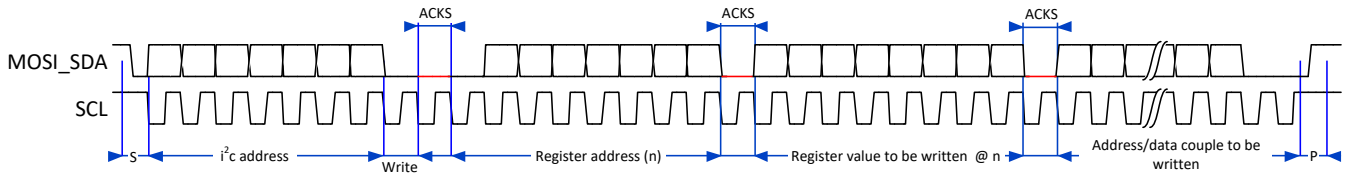


Figure 6-1: I2C write (multiple transactions)

To access registers in read mode, first address should first be send in write mode. Then a stop and a start conditions must be generated and data bytes are transferred with automatic address increment:

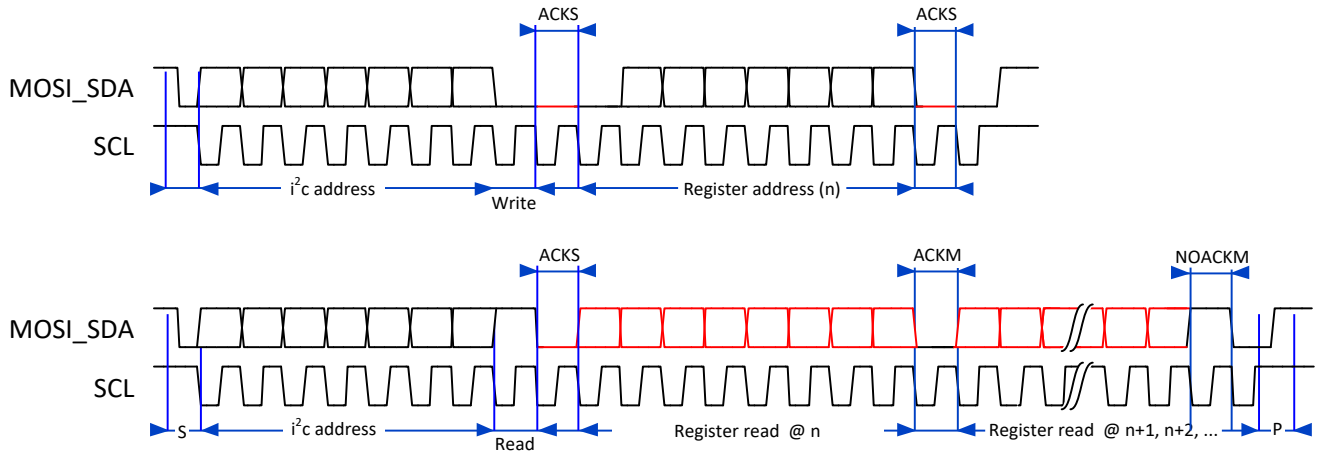


Figure 6-2: I2C read (multiple transactions)

In the case of a read transaction, it is possible to avoid stopping and starting again a new transaction by following the register address with a repeated start.

6.2. SPI INTERFACE

The SPI interface is a standard Serial to Peripheral Interface. It is compatible with two of the four standard transmission modes. The automatic selection between the two modes ([CPOL='0' and CPHA='0'] and [CPOL='1' and CPHA='1']) is determined by the value of SCL after the CS rising edge.

The SPI interface can be used in 4-wire or 3-wire. The 3-wire is selected by setting the register *reg_spi_i2c_cfg.spi_3w_en* to '1'. The pin MOSI is used as a data pin in 3-wire mode.

The SPI interface is a byte-oriented transmission interface. The first byte sent is contains the address of the register and access type of the transmission – on the first transmitted bit (reads register – '1' – or writes register – '0'). The following bytes contain register values. On read access the address read is incremented for each additional byte until address 0x7F. When reaching this address, the devices internal address counter wraps to 0x00 and starts to read again from this address.

In case of a write transaction the protocol is based on an interleaved scheme of address and data. The first byte contains a 7-bit address and the write command (First sent bit of the first byte equal to '0'). The second byte contains data to be written to this address.

It is important to note that it is possible to send a set of write commands, followed by a multi read transaction within the same SPI transaction. Once in read mode, write accesses are not possible anymore in the same SPI transaction.

The following example shows a write of some registers followed by a check of the data.

0x00	0x05	0x01	0x03	0x06	0x02	0x80	0x00	0x00	0x00	0x00
Set hrv_period to 1/8 Hz		Set hrv_meas to 128ms		Set the system in primary cell mode		Read registers 0x00 to 0x03				

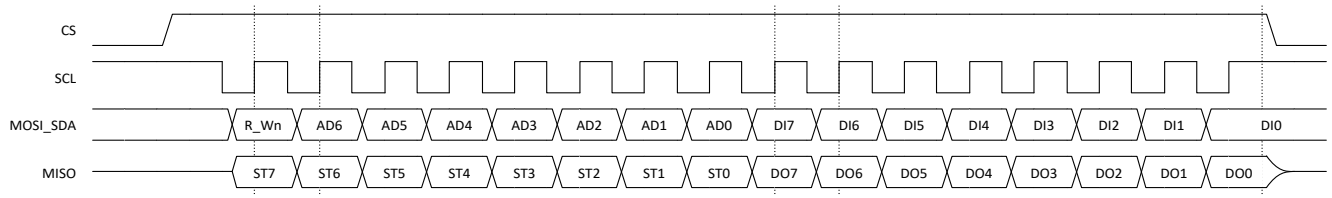


Figure 6-3 SPI transaction scheme CPOL=1, CPHA=1

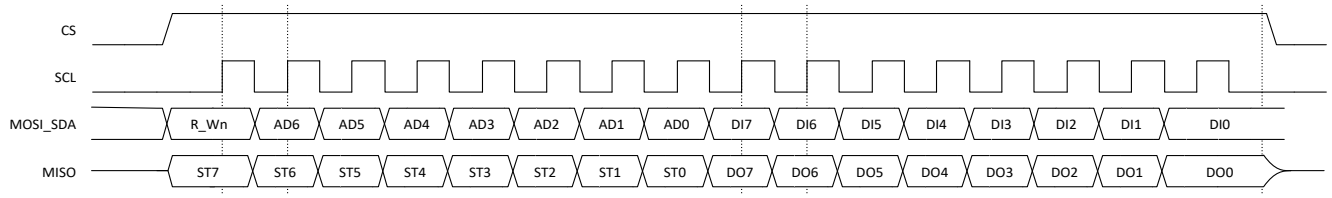


Figure 6-4 SPI transaction scheme CPOL=0, CPHA=0

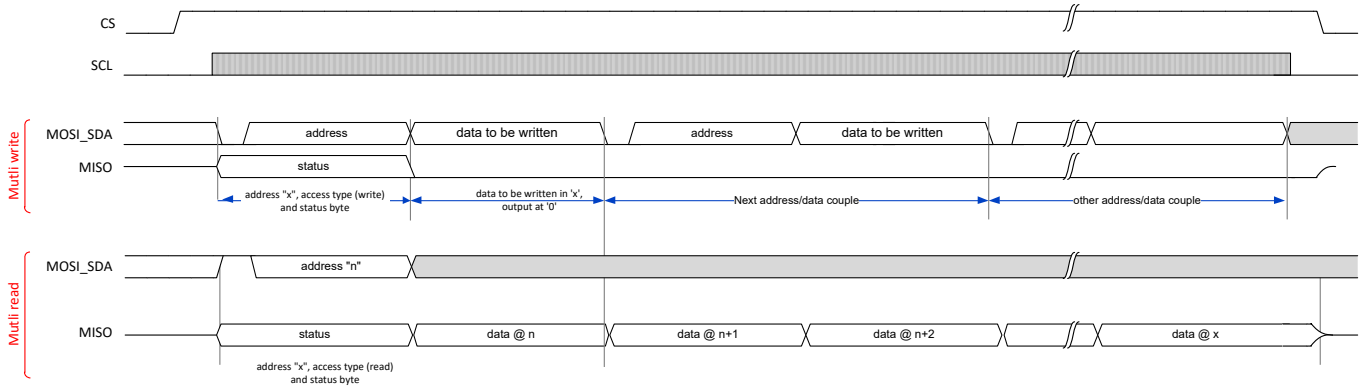


Figure 6-5 Multi register access transaction

Along with the address information the SPI interface sends the status register (*reg_status* – address 0x22) as the first response byte. In the case of the 3-wire mode the protocol is identical to the I²C interface, and doesn't allow having the status byte when sending the address to the device.

Interface signals are the following:

- CS chip select, active high
- SCL clock
- MOSI_SDA data input; data input/output in 3-wire mode
- MISO data output; Hi-Z level in 3-wire mode

6.2.1. INTERFACE SELECTION

The interface selection process is done through the use of the CS pin.

At reset (at the end of the boot sequence) the default interface selection is I²C. The SPI selection is done by asserting the CS pin. After CS assertion the SPI interface is selected until the device is shut-down (V_{STS} below V_{cs_lo}).

If the CS pin is continuously asserted (through a hard connection to VSUP) the SPI interface is permanently selected. I²C is not available in this case.

Register name: reg_spi_i2c_cfg			Address: 0x18	Default value mapped in E²PROM
Bits	**Bit name**	**Type**	**Description**	
7	spi_3w_en	RW	Set the SPI in its 3 wire mode (shared MOSI/MISO)	
6:0	i2c_addr	RW	i2c address	

Table 6-1 SPI/I2C configuration register (0x18)

6.3. E2PROM

6.3.1. ACCESSING THE E2PROM

The on-chip E²PROM contains the default working parameters of the device. The E²PROM address space is mapped into the EM8504 register map from address 0x40 (E²PROM address 0) to 0x7F ((E²PROM address 63). Some addresses are reserved (0x76 to 0x7F) and are accessible in read-only mode by the user; some contain the defaults values – as described on §8. All other addresses can be freely used.

The user can write on the E²PROM at any time. Note that no protection is built in to prevent an incomplete write transaction caused by a lack of energy (STS too low). The user must ensure that the EM8504 is able to properly finish a write transaction.

Read and write accesses are performed through the serial interface. In difference to standard registers (addresses 0x00 to 0x3F), an E²PROM access requires a dead time. A read access needs a dead time between read address and the data. A write access requires a dead time after having sent the write data.

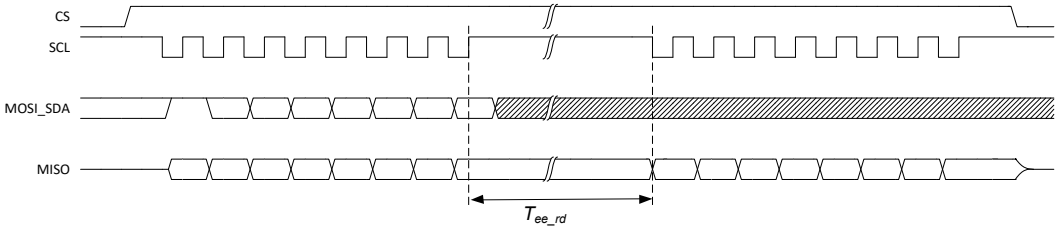


Figure 6-6 SPI transaction for reading the E²PROM (CPOL=1)

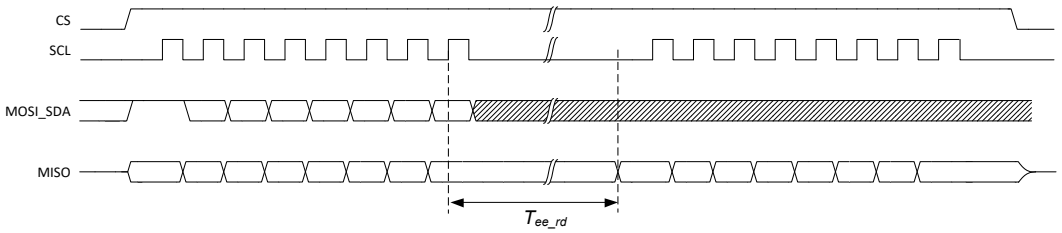


Figure 6-7 SPI transaction for reading the E²PROM (CPOL=0)

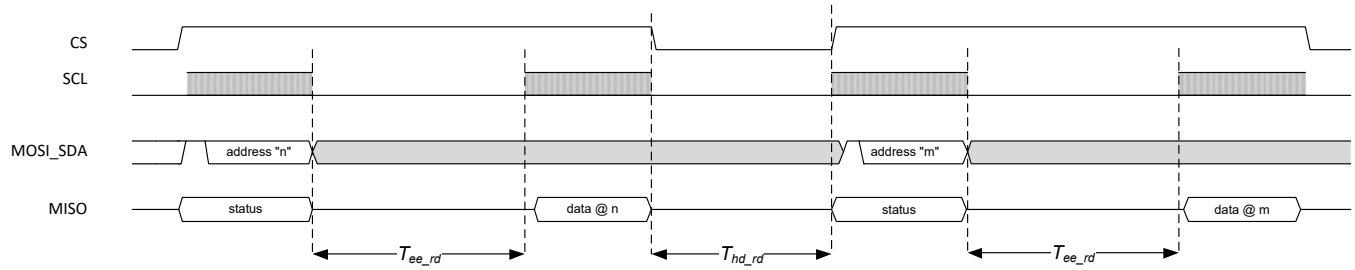


Table 6-2 SPI multiple E²PROM read transactions

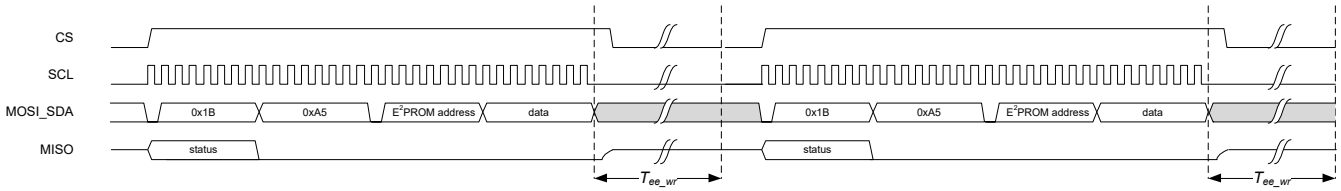


Figure 6-8 Two consecutive single E²PROM write SPI transactions

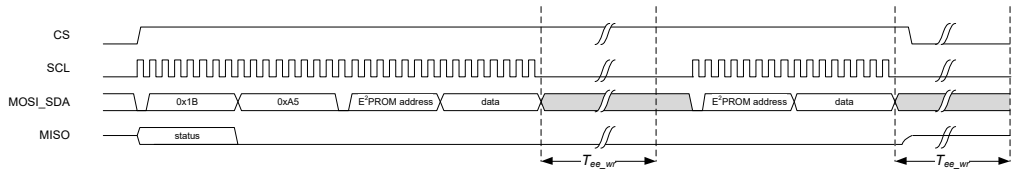


Figure 6-9 SPI multi-byte transaction for writing the E²PROM

When the I²C serial interface is used, only a single action per transaction is allowed when accessing the E²PROM. As for an SPI transaction, a dead time is necessary. Prior to a write transaction into the E²PROM it is necessary to set the *reg_protection_key* register to 0xA5.

For a write transaction, no other I²C transaction into the E²PROM address area is allowed for T_{wr_ee} after the end of the write transaction. A transaction inside this time window is ignored by the device.

In the following diagram, responses from EM8504 are shown in red, data from the I²C master in black.

The following abbreviations are used:

- W Write transaction request
- R Read transaction request
- S Start an I²C transaction
- P Stop an I²C transaction
- A I²C Acknowledge
- N I²C Non Acknowledge

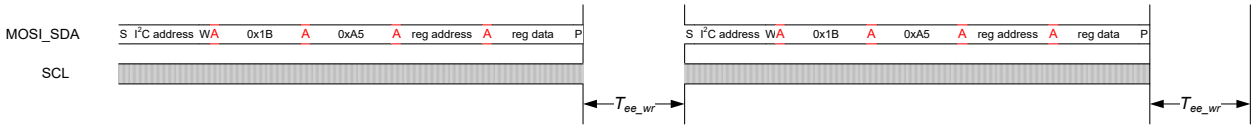


Figure 6-10 I²C transaction for writing on the E²PROM

For a read transaction a dead-time (T_{rd_ee}) has to be inserted in between the address setting transaction and the read action itself.

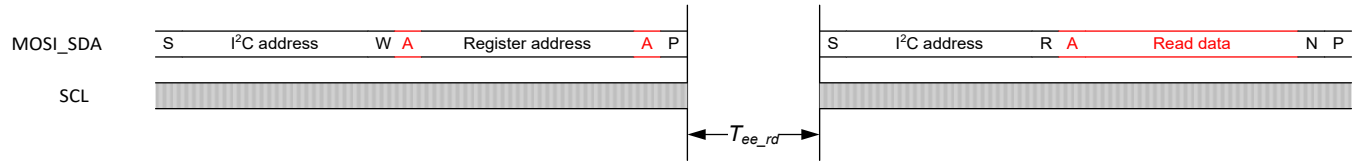


Figure 6-11 I²C transaction for reading the E²PROM

7. TYPICAL CHARACTERISTICS

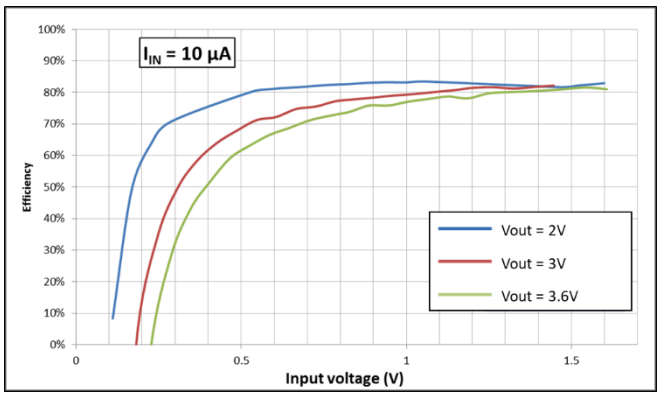


Figure 7-1 Charger Efficiency vs Input Voltage (I_{IN} = 10µA)

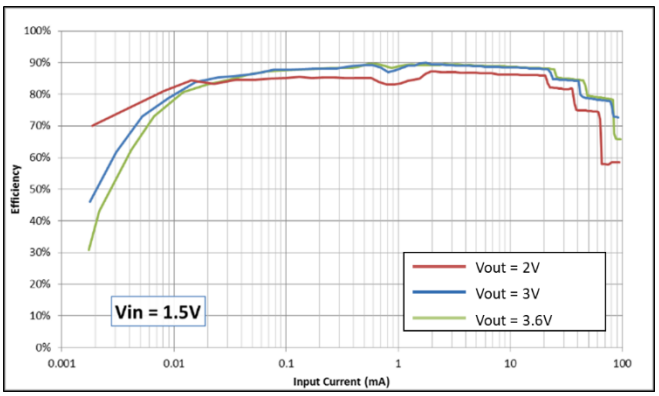


Figure 7-2 Charger Efficiency vs Input Current (V_{IN} = 1.5V)

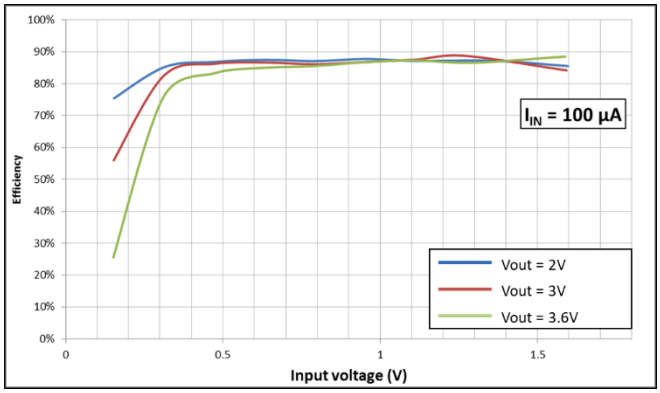


Figure 7-3 Charger Efficiency vs Input Voltage (I_{IN} = 100µA)

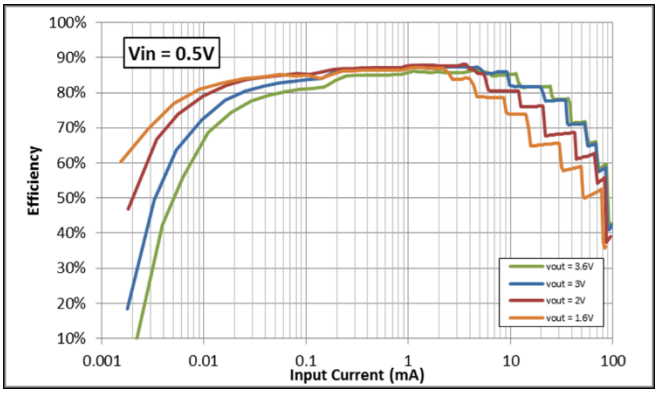


Figure 7-4 Charger Efficiency vs Input Current (V_{IN} = 0.5V)

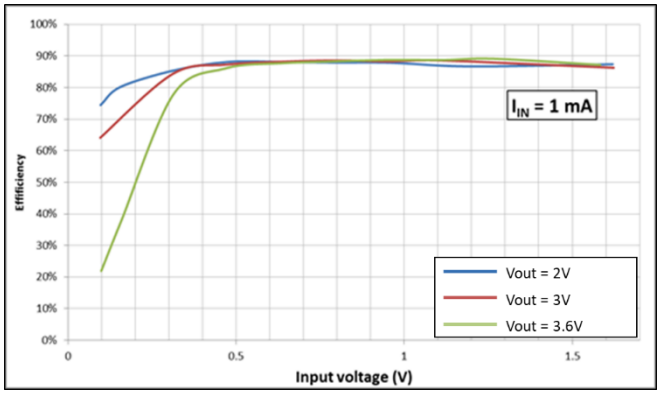


Figure 7-5 Charger Efficiency vs Input Voltage (I_{IN} = 1mA)

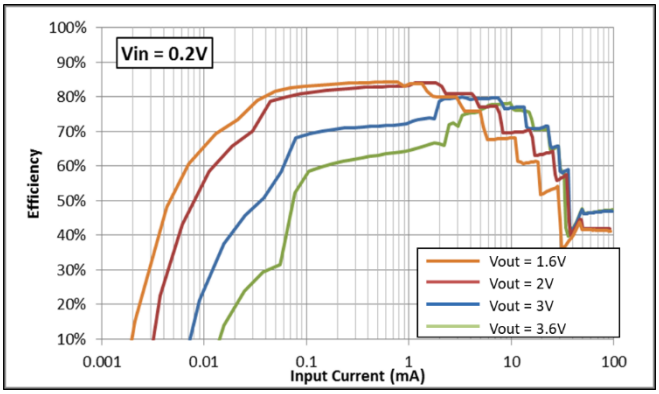


Figure 7-6 Charger Efficiency vs Input Current (V_{IN} = 0.2V)

8. REGISTER MAP

Area	Register Name	Address		Factory	Index							
		DEC	HEX	Value	7	6	5	4	3	2	1	0
Configuration registers with default value in E²PROM	reg_t_hrv_period	0	0x00	0x05	-	-	-	-	-	t_hrv_period(2:0)		
	reg_t_hrv_meas	1	0x01	0x00	-	-	-	-	-	t_hrv_meas(2:0)		
	reg_t_sts_period	2	0x02	0x07	-	-	-	-	-	t_sts_period(2:0)		
	reg_t_lts_period	3	0x03	0x04	-	-	-	-	-	t_lts_period(2:0)		
	reg_v_hrv_cfg	4	0x04	0x01	-	hrv_check_vld	v_hrv_min(5:0)					
	reg_hrv_check_lvl	5	0x05	0x04	-	-	-	-	hrv_check_lvl(3:0)			
	reg_lts_cfg	6	0x06	0x00	-	-	-	-	-	prim_cell_connect	prim_cell	no_bat_protect
	reg_v_bat_max_hi	7	0x07	0x38	-	-	v_bat_max_hi(5:0)					
	reg_v_bat_max_lo	8	0x08	0x37	-	-	v_bat_max_lo(5:0)					
	reg_v_bat_min_hi_dis	9	0x09	0x28	-	-	v_bat_min_hi_dis(5:0)					
	reg_v_bat_min_hi_con	10	0x0A	0x28	-	-	v_bat_min_hi_con(5:0)					
	reg_v_bat_min_lo	11	0x0B	0x27	-	-	v_bat_min_lo(5:0)					
	reg_v_apl_max_hi	12	0x0C	0x2D	-	-	v_apl_max_hi(5:0)					
	reg_v_apl_max_lo	13	0x0D	0x2C	-	-	v_apl_max_lo(5:0)					
	reg_ldo_cfg	14	0x0E	0x45	vsup_tied_low	v_vaux_ldo(2:0)			frc_ulp_ldo	v_ulp_ldo(2:0)		
	reg_pwr_cfg	15	0x0F	0x00	-	dis_vaux_gnd2_hrv_low	dis_vaux_gnd1_hrv_low	dis_vaux_gnd0_hrv_low	dis_vaux2_hrv_low	dis_vaux1_hrv_low	dis_vaux0_hrv_low	dis_vsup_hrv_low
	reg_vaux_cfg	16	0x10	0x00	-	-	vaux2_cfg(1:0)		vaux1_cfg(1:0)		vaux0_cfg(1:0)	
	reg_vaux_gnd_cfg	17	0x11	0x00	-	-	-	-	-	vaux_gnd2_cfg	vaux_gnd1_cfg	vaux_gnd0_cfg
	unused	18	0x12	0x0C	-	-	-	-	-	-	-	-
	reg_ext_cfg	19	0x13	0x61	sda_slopectrl	-	-	-	-	-	-	-
	unused	20	0x14	0xE8	-	-	-	-	-	-	-	-
	unused	21	0x15	0x03	-	-	-	-	-	-	-	-
	unused	22	0x16	0x00	-	-	-	-	-	-	-	-
	reg_t_hrv_low_cfg	23	0x17	0x25	-	t_hrv_low_period(2:0)			-	t_lts_hrv_low_period(2:0)		
	reg_spi_i2c_cfg	24	0x18	0x77	spi_3w_en	i2c_addr(6:0)						
	reg_pwr_mgt	25	0x19	0x00	frc_prim_dcdc_dis	vaux_gnd2_en	vaux_gnd1_en	vaux_gnd0_en	vaux2_en	vaux1_en	vaux0_en	-
No EPROM default value	reg_soft_res_word	26	0x1A	0x00	soft_res_word(7:0)							
	reg_protect_key	27	0x1B	0x00	protect_key(7:0)							
	reg_lux_meter_cfg	28	0x1C	0x00	-	lux_auto_meas	lux_auto_rng	lux_manu	lux_lvl(3:0)			
	reg_lux_meter_result	29	0x1D	0x00	-	-	-	lux_meter_busy	lux_meter_result(3:0)			
	reg_status	34	0x22	0x00	eeprom_data_busy	hrv_lux_busy	hrv_low	bat_low	sw_vdcdc_lts_nsts	sw_lts_sts	hrv_dis	lts_protect
	reg_vld_status	35	0x23	0x00	lts_bat_min_hi	lts_bat_min_lo	sts_bat_max_hi	sts_bat_max_lo	sts_apl_max_hi	sts_apl_max_lo	sts_bat_min_hi	sts_bat_min_lo
E²PROM Values	eeprom0	64	0x40	0x05	-	-	-	-	-	t_hrv_period(2:0)		
	eeprom1	65	0x41	0x00	-	-	-	-	-	t_hrv_meas(2:0)		
	eeprom2	66	0x42	0x07	-	-	-	-	-	t_sts_period(2:0)		
	eeprom3	67	0x43	0x04	-	-	-	-	-	t_lts_period(2:0)		
	eeprom4	68	0x44	0x01	-	hrv_check_vld	v_hrv_min(5:0)					
	eeprom5	69	0x45	0x04	-	-	-	-	hrv_check_lvl(3:0)			
	eeprom6	70	0x46	0x00	-	-	-	-	-	prim_cell_connect	prim_cell	no_bat_protect
	eeprom7	71	0x47	0x38	-	-	v_bat_max_hi(5:0)					
	eeprom8	72	0x48	0x37	-	-	v_bat_max_lo(5:0)					
	eeprom9	73	0x49	0x28	-	-	v_bat_min_hi_dis(5:0)					
	eeprom10	74	0x4A	0x28	-	-	v_bat_min_hi_con(5:0)					
	eeprom11	75	0x4B	0x27	-	-	v_bat_min_lo(5:0)					
	eeprom12	76	0x4C	0x2D	-	-	v_apl_max_hi(5:0)					
	eeprom13	77	0x4D	0x2C	-	-	v_apl_max_lo(5:0)					
	eeprom14	78	0x4E	0x45	vsup_tied_low	v_vaux_ldo(2:0)			frc_ulp_ldo	v_ulp_ldo(2:0)		
	eeprom15	79	0x4F	0x00	-	dis_vaux_gnd2_hrv_low	dis_vaux_gnd1_hrv_low	dis_vaux_gnd0_hrv_low	dis_vaux2_hrv_low	dis_vaux1_hrv_low	dis_vaux0_hrv_low	dis_vsup_hrv_low
	eeprom16	80	0x50	0x00	-	-	vaux2_cfg(1:0)		vaux1_cfg(1:0)		vaux0_cfg(1:0)	
	eeprom17	81	0x51	0x00	-	-	-	-	-	vaux_gnd2_cfg	vaux_gnd1_cfg	vaux_gnd0_cfg
	eeprom18	82	0x52	0x0C	-	-	-	-	-	-	-	-
	eeprom19	83	0x53	0x61	sda_slopectrl	-	-	-	-	-	-	-
	eeprom20	84	0x54	0xE8	-	-	-	-	-	-	-	-
	eeprom21	85	0x55	0x03	-	-	-	-	-	-	-	-
	eeprom22	86	0x56	0x00	-	-	-	-	-	-	-	-
	eeprom23	87	0x57	0x25	-	t_hrv_low_period(2:0)			-	t_lts_hrv_low_period(2:0)		
	eeprom24	88	0x58	0x77	spi_3w_en	i2c_addr(6:0)						
	eeprom25	89	0x59	0x00	frc_prim_dcdc_dis	vaux_gnd2_en	vaux_gnd1_en	vaux_gnd0_en	vaux2_en	vaux1_en	vaux0_en	-

Table 8-1 Register Map

9. TYPICAL APPLICATIONS

9.1. SAMPLE SCHEMATICS

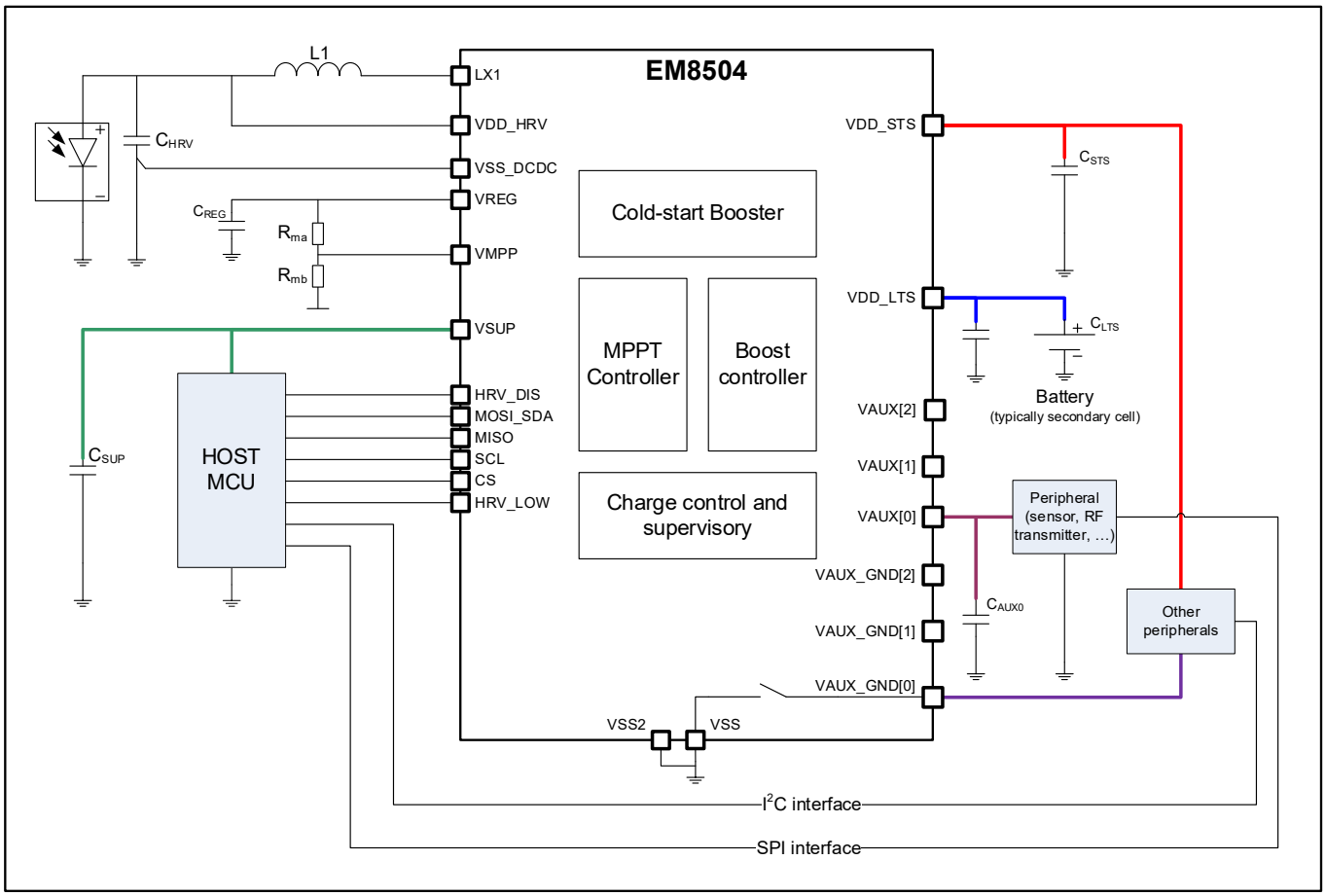


Figure 9-1 Example of Application with a Solar Cell Harvester

Component	Symbol	Value
Booster inductor	L1	47µH
Harvester capacitor	C_{HRV}	4.7µF
MPP bridge resistor up	Rma	See section 5.2.4
MPP bridge resistor down	Rmb	See section 5.2.4
STS capacitor	C_{STS}	47µF
Regulator capacitor	C_{REG}	470 nF
Main supply output capacitor	C_{SUP}	1 µF
Auxiliary (2) supply output capacitor	C_{AUX2}	1 µF

Table 9-1 Component list for solar cell application

9.2. INDUCTOR SELECTION

The boost DCDC converter requires a properly selected inductor to obtain highest efficiency. Apart from the typical value of the inductor (47 µH ± 20%), coil saturation current and the internal resistivity need to be considered.

The saturation current should be at least 30% higher than the maximum peak current. The internal resistivity should be as low as possible – a typical value of 0.65 Ω is suitable.

9.2.1. REFERENCE INDUCTORS

Manufacturer	Size			RDC		Part number	Comments
	Length	Width	Thickness	Typ	Max		
TDK	4mm	4mm	2.4mm	560mΩ	644mΩ	VLCF4024T-470MR44-2	High efficiency performances
TDK	3mm	3mm	1.2mm	1.25Ω	1.5Ω	VLS3012ET-470M	
TAIYO YUDEN	1.6mm	0.8mm	0.8mm	2.5Ω		CBMF1608T470K	Up to 500uW and Vhrv 1V max

Table 9-2 List of reference inductors

9.3. CAPACITOR SELECTION

The selection of the capacitor is strongly linked to the hysteresis value set in the configuration registers. Please refer to the application notes for capacitors values for different system applications scenarios.

10. ORDERING INFORMATION

Part Nb	Package form	Delivery form	Quantity
EM8504-V007-LF24B+	QFN24 4x4 mm	Tape & Reel	2'500
EMEVB8504	Evaluation Board	Box	1

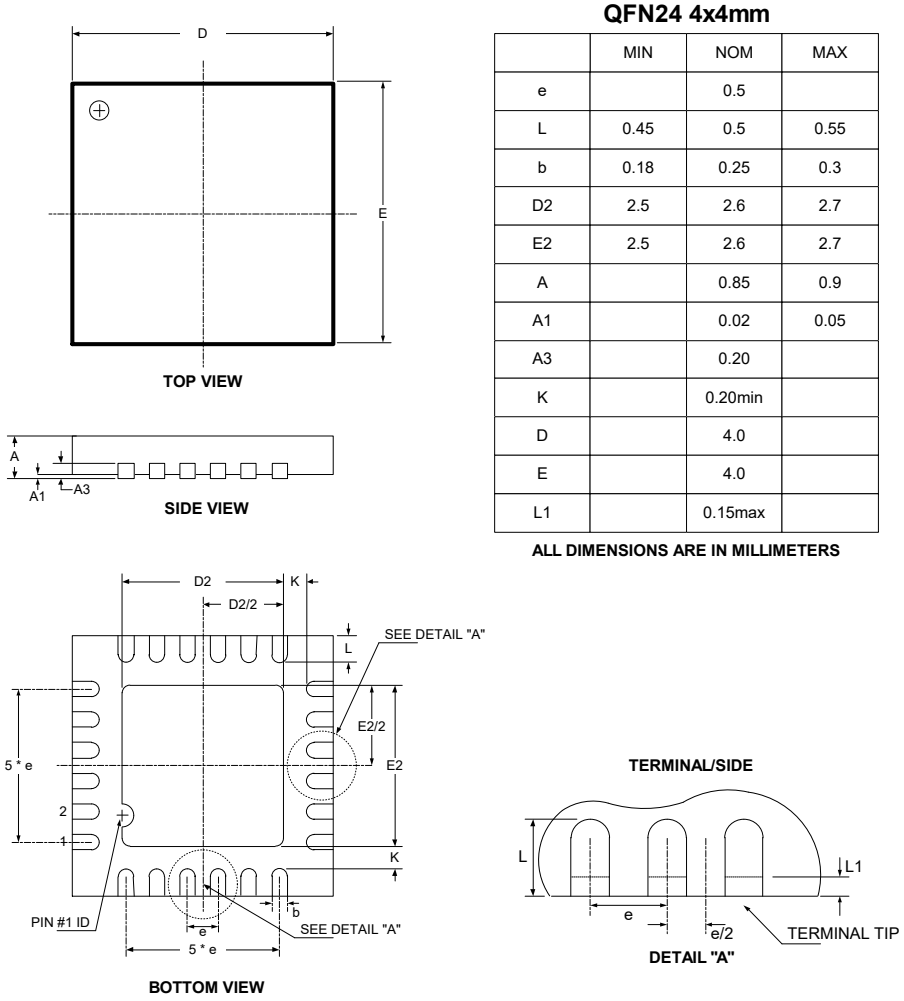
Table 10-1 Ordering Information

For other delivery format please contact EM Microelectronics representative.

11. PACKAGE INFORMATION

11.1. QFN24 4X4 PACKAGE

Package in tape & reel; shelf life is 12 months.



QFN24 4x4mm

	MIN	NOM	MAX
e		0.5	
L	0.45	0.5	0.55
b	0.18	0.25	0.3
D2	2.5	2.6	2.7
E2	2.5	2.6	2.7
A		0.85	0.9
A1		0.02	0.05
A3		0.20	
K		0.20min	
D		4.0	
E		4.0	
L1		0.15max	

ALL DIMENSIONS ARE IN MILLIMETERS

Figure 11-1 QFN24 Mechanical Information

11.1.1. PACKAGE MARKING

This section reports the package marking for EM8504. Additional marking letters and numbers are used for lot traceability.

8	5	0	4	0
0	7			A