ULTRA LOW POWER ENHANCED LCD & LED CONTROLLER AND DRIVER WITH MULTI FORMAT CHARACTER GENERATOR

Description

EM6127 is a controller and driver for graphic or character monochrome TN – Twisted Nematic, STN – Super-Twisted Nematic and Filtered STN LCD displays. Several EM6127 integrated functions save system power needs. The enhanced EM6127 driver displays different character or bitmap formats. Various effects are available such as scrolling, reverse, blinking and more are available. In addition, the controller is able to display ROM-defined or RAM custom-made messages. EM6127 can start in user-defined modes and configurations.

The EM6127 is an extremely low power LCD controller and driver product. The typical current consumption is typically 20 µA in MUX 32 configuration with internally generated VLCD and external capacitors.

The one character line, active addressing mode is an important feature of the EM6127. It provides significant improvement in current consumption. The typical current consumption in this mode is only 5 µA.

The 5x7 character format can be zoomed 2 or 3 times (10x14 and 15x21), such that a large date can be displayed, for example.

Features

- Max. addressable matrix: 32 rows x 101 columns
- Slim IC for Chip-On-Film, Glass or Plastic technologies (COF, COG, COP)
- VDD supply voltage:
  - Low voltage configuration: 1.2V to 2V
  - Standard configuration: 2V to 3.6 V
- Power consumption:
  - Full matrix mode, 20 µA with internally generated VLCD and external capacitors
  - One character line mode, 5 µA with internally generated VLCD and external capacitors
- I^2C interface and Serial bus interface
- R/W Internal Display Data RAM for characters
- Character Generator RAM: 16 characters or bitmap
- Character Generator ROM: 240 characters or bitmap
- Programmable characters or bitmap font format:
  - 5x7, 6x8, 5x10, 10x16, 15x24
- Personalization of ROM – define your own characters
- Programmable Multiplex rates:
  - static, 2, 3, 4, 8,10,16, 20, 24, 32
- 16 different predefined display modes in ROM
- Full bitmap mode
- Horizontal and vertical scrolling by dot with four selectable speeds of scrolling
- Full and partial scrolling
- Reverse mode display
- Inverse mode for character or line
- Blink (four frequencies and four duty cycles) for character or line
- Programmable cursor: XOR, OR, AND operations
- Characters superposition function
- Four sequences of sixteen characters max. available
- 64 predefined messages in ROM and 16 messages in RAM
- Partial display mode and one character line mode
- LCD supply voltage VLCD internally generated and digitally programmable in 127 steps from 1.25V to 7.6V; external VLCD possible
- Selectable 1, 2, 3, 4, 5 voltage multiplier factor for VLCD
- Selectable bias voltages generation
- Oscillator for LCD refresh
- LED driver for back or front light illumination, with two independent outputs and external adjustable current limitation
- LED supply voltage internally generated and digitally programmable by 31 steps from 3.7V to 5.25V; external VLED possible
- Selectable temperature coefficient for LCD thermal compensation
- High noise immunity on inputs
- Operation temperature range: -40°C to +85°C

Applications

- Battery powered devices
- Printers and Fax
- Weigh scale, utility meters
- Point-of-sale terminals
- Home appliances

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1 BLOCK DIAGRAM

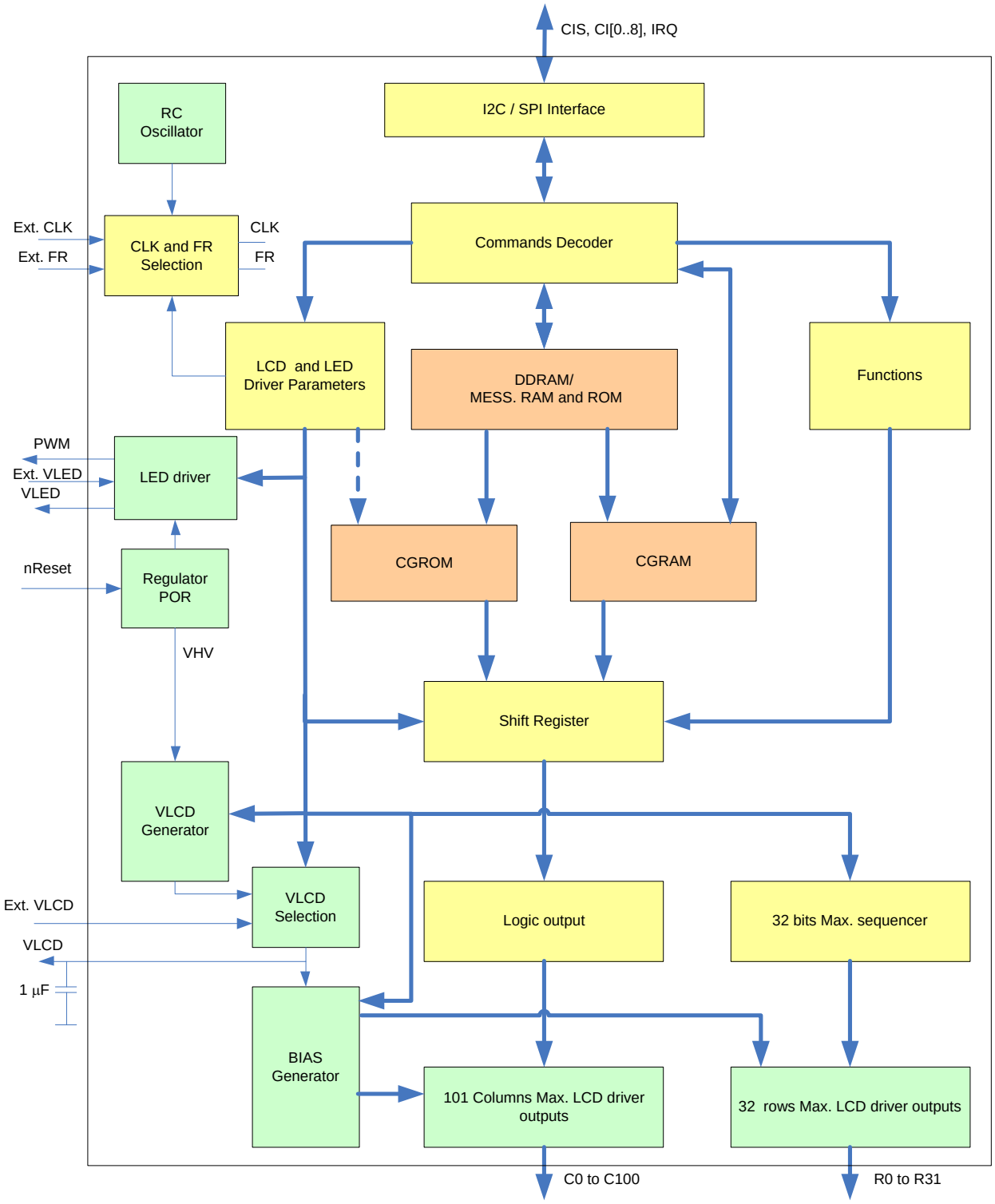


Figure 1 EM6127 Block diagram

2 ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	VDD	-0.3 to + 3.8 V
Voltage at VLCD	VLCD	-0.3 to + 8 V
All input voltages	VLogic	-0.3 to VDD + 0.3 V
Voltages at R0 to R31 And C0 to C100	VDisplay	-0.3 to VLCD + 0.3 V
Storage temperature	Tstore	-65 to 150°C
Electrostatic discharge to Mil-Std-883C method 3015.7 with ref. to VSS	Vhbm	+/- 2000 V
Maximum soldering conditions	TSmax	250°Cx10s

Table 1 Absolute Maximum Ratings

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

2.2 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

2.3 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Logic supply voltage (1) “HSV”	VDD	2	3.6	V
Logic supply voltage (2) “LSV”	VDD	1.2	2	V
LCD supply voltage	VLCD	1.25	7.6	V
Temperature range	TA	-40	85	°C

(1) Standard configuration
(2) Low voltage configuration

2.4 Electrical Characteristics

Unless otherwise specified: V_{DD}= 1.2V to 3.6V, T_A = -40 to +85°C. Typical numbers at T_A = +25°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current						
Supply current on VDD, Standard configuration	IDD_1	Disable mode (Note 1)		50		nA
		Sleep mode (Note 1)		750		nA
		LCD full matrix on, mode 4 (Note 2)		22		µA
		LCD full matrix on, mode 3 (Note 2)		25		µA
		Static one character line mode (Note 3)		5		µA
		One character line mode with blink and scroll (Note 3)		8.3		µA
		LED driver on, LCD off (Note 4)		35		µA
		LCD full Matrix on, Mode 3, external VLCD (Note 5)		9		µA
		LED driver on, LCD off, external VLED (Note 6)		3.1		µA
Supply current on VDD, Low voltage configuration	IDD_2	Disable mode (Note 1)		100		nA
		Sleep mode (Note 1)		160		nA
		LCD full matrix on, mode 4 (Note 2)		39		µA
		LCD full matrix on, mode 3 (Note 2)		42		µA
		Static one character line mode (Note 3)		6		µA
		One character line mode with blink and scroll (Note 3)		10		µA
		LED driver on, LCD off (Note 4)		150		µA
		LCD full Matrix on, Mode 3, external VLCD (Note 5)		8.3		µA

		LED driver on, LCD off, external VLED (Note 6),		3.7		µA
Control Input Signals						
Input leakage	IIN	Vi=VSS or VDD	-1		1	µA
Low level input voltage	VIL				0.2xVDD	V
High level input voltage	VIH		0.8xVDD			V
LCD Outputs						
Internally generated LCD supply voltage Standard voltage reference (AVREF=0)	VLCD	VLCD = 0000000h		1.25		V
		VLCD = 1111111h		7.6		V
VLCD step between two consecutive programmed VLCD levels Standard voltage reference (AVREF=0)	VLCD step			50		mV
Internally generated LCD supply voltage Low power voltage reference (AVREF=1)	VLCD	VLCD = 0000000h		0.625		V
		VLCD = 1111111h		3.6		V
VLCD step between two consecutive programmed VLCD levels Standard voltage reference (AVREF=1)	VLCD step			25		mV
V bias tolerance	V bias tol. (Note 7)		-80		80	mV
LED Outputs						
Internally generated LED supply voltage	VLED	VLD = 00000h		3.7		V
		VLD = 11111h		5.25		V
VLED step between two Consecutive programmed VLED levels	VLED step			50		mV
Voltage drop of output switch for LED	ΔV(PWMi (i=1or 2)	VLED = 4.5 V ILED = 3 mA			200	mV

Table 2 Electrical Characteristics

Note 1: The conditions are the following:
- VDD: 3.0 V for standard configuration and 1.5 V for low voltage configuration

Notes 2 to 6: typical values for supply current may change depending on display load.

Note 2: The conditions are the following:
- VDD: 3.0 V for standard configuration and 1.5 V for low voltage configuration
- VLCD: 5.0 V, FR=111, Mux 32, LCD filled with command Autodisplay
- In HSV mode, the internal voltage multiplier factor is 2; in LSV mode, this factor is 4

Note 3: The conditions are the following:
- VDD: 3.0 V for standard configuration and 1.5 V for low voltage configuration
- VLCD: 1.5 V, Active addressing, LCD filled with command Autodisplay, Mode 0
- Low power voltage reference, minimal frequency, ADIS_RD=1 for static mode only

Note 4: The conditions are the following:
- VDD: 3.0 V for standard configuration and 1.5 V for low voltage configuration
- Internal generated VLED: 4.5 V, L1DC=3, L2DC=3

Note 5: The conditions are the following:
- VDD: 3.0 V for standard configuration and 1.5 V for low voltage configuration
- External VLCD set to 5.0V, FR=111, Mux 32, LCD filled with command Autodisplay

Note 6: The conditions are the following:
- VDD: 3.0 V for standard configuration and 1.5 V for low voltage configuration
- External VLED set to 4.5V, L1DC=3, L2DC=3

Note 7: The Vbias tol = Vi – Vi theoretic (see Table 6 Bias ratio) where Vi are the intermediate voltages.

2.5 Timing Characteristics

Unless otherwise specified: V_{DD}= 1.2V to 3.6V, T_A = -40 to +85°C. Typical numbers at T_A = +25°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Startup timing characteristics						
Start-up time (Low voltage configuration)				2		ms
Start-up time (Standard configuration)				5		ms
Start-up time after Sleep command				300		us
I2C timing characteristics						
SCL frequency	fI^{2}c				400	kHz
SCL low period	tLOW		1150			ns
SCL high period	tHIGH		850			ns
SDA setup time	tSDASU		100			ns
SDA hold time	tSDAH		0			ns
SCL and SDA rise time	tR				400	ns
SCL and SDA fall time	tF				100	ns
Setup time for a repeated start condition	tSURSTA		1150			ns
Hold time for a start condition	tHSTA		850			ns
Setup time for a stop condition	tSUSTO		850			ns
Spike width on SCL and SDA	tSW				10	ns
Time before a new transmission can start	tBUF		1150			ns
Serial bus timing characteristics						
SCK frequency	fSPI				1	MHz
SCK low period	tSCL			500		ns
SCK high period	tSCH			500		ns
SDI setup time	tSDISU		100			ns
SDI hold time	tSDIH		60			ns
SDO setup time	tSDOH				100	ns
SCK rise time	tSCR				50	ns
SCK fall time	tSCF				50	ns
nSS setup time	tNCSSU		400			ns
nSS hold time	tNCSH		400			ns
Time before a new transmission can start, nSS minimum high time	tSPBUF		400			ns
LED driver frequency						
PWM frequency	fPWM			Fref/2560		Hz

Table 3 Timing characteristics

2.6 Timing Characteristics and Timing Diagrams

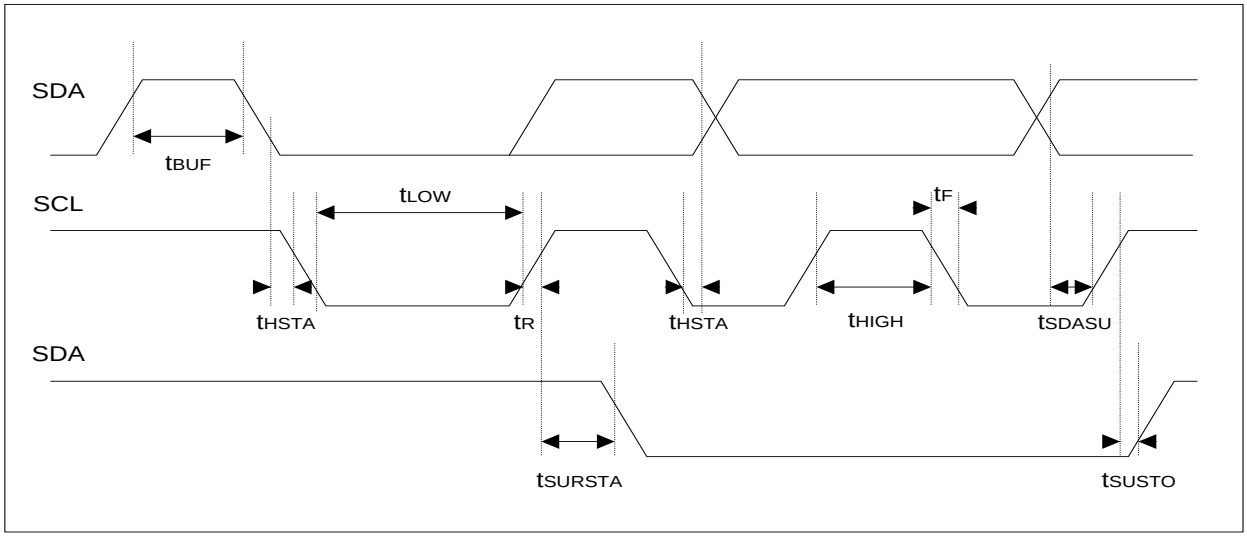


Figure 2 I²C timing diagram

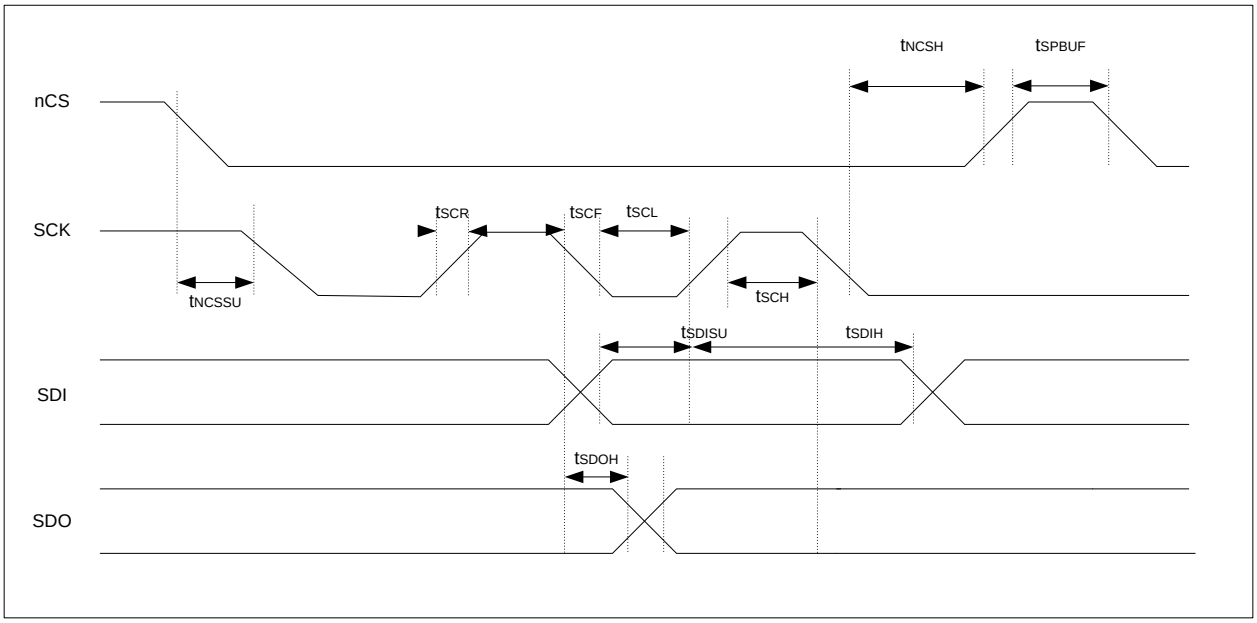


Figure 3 SPI timing diagram

3 TYPICAL APPLICATION

In normal use in a pre-defined mode, the instructions, to be sent via serial interface after start-up, are reduced to the minimum.

Automatic address increment by 1 of internal RAM addresses during serial communication reduces the host processor load as well.

As an example, to write 4 lines of 17 characters in mode 1, the following commands have to be sent:

Step	Commands to be sent by host processor	Actions done by the LCD driver
1	*Power on display*	*Power up all circuits parts* *Reset all registers* *Configure all parameters: mode parameters, VLCD, Temperature coefficient, bias ratio, number of multiplier stages, clock, charge pump frequency, frame frequency (data stored in EEPROM)* *Display Control with bit ON (data stored in EEPROM)* *Set DDRAM to 0 (Automatic increment is enabled and DDRAM is selected by default)*
2	*Write data:* Write data command followed by 4 x 17 data	*Display data*

Table 4 Typical application commands

4 SPECIAL APPLICATION

It is possible to drive bigger LCD (202 columns x 32 rows) by connecting two EM6127 drivers in parallel. The connection should be as follows:

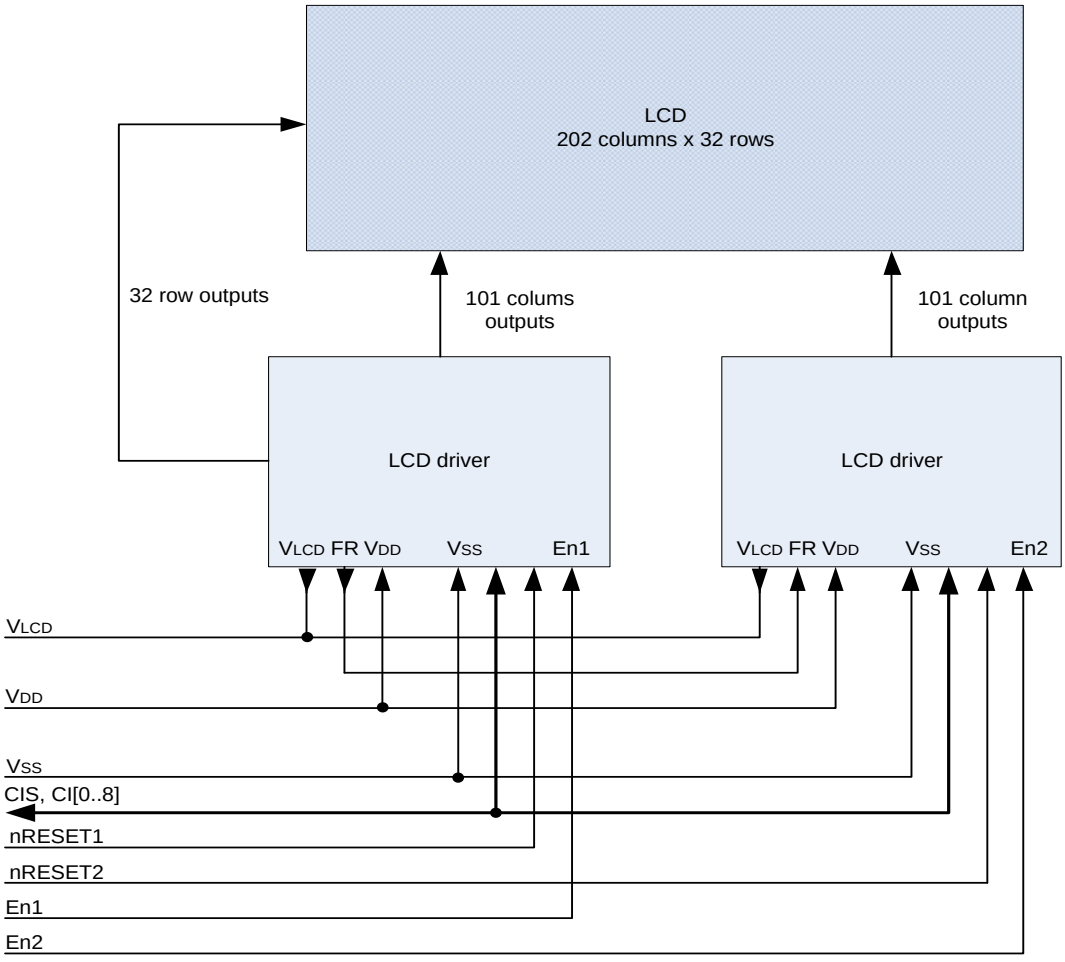


Figure 4 Driving double size LCD

5 PIN DESCRIPTION

Pin	Pin Name	Type	Description
130	EN	I	Chip enable (see notes below)
129	N_RST	I	External Reset, active low
125	LSV	I	Low Supply Voltage selection input (see notes below)
140, 139	CBH, CBL	I/O	External capacitor for low voltage configuration
138	VCP	Power	Charge pump voltage output for low voltage configuration. Connect to VDD in standard configuration.
159-174, 98-113	R0 to R31	O	LCD row driver outputs, connected to LCD common electrodes
175-178, 1-97	C0 to C100	O	LCD column driver outputs, connected to LCD segment electrodes
135	VDD	Power	Main supply voltage input (see notes below)
136	VDDC	Power	Supply voltage for current source (see notes below)
124	VSSD	Ground	Ground supply for logic part
123	VSSA	Ground	Ground supply for analog part
141, 142	VSSP[1:0]	Ground	Ground supply for power part (voltage multiplier and booster). Two pads for better drive capability.
137	VDDA	Power	Analog regulator output, capacitor connection
128	VDDD	Power	Digital regulator output for standard configuration. Connect to VDD in low voltage configuration
158	VLCD_IN	Power	External LCD supply voltage input (see notes below)
157	VLCD_OUT	Power	Internal LCD supply voltage output (see notes below)
156	PWM1	O	PWM output for back light or front light LED 1
154	PWM2	O	PWM output for back light or front light LED 2
146, 148	SW[1:0]	O	Switch for LED driver inductor. Two pads for better drive.
150, 152	VLED[1:0]	O	LED regulated voltage
126	CIS	I	I^2C/SPI interface selection. If this signal is high, the I2C interface is selected.
117	CIO0/SCL/SCK	I/O	I^2C clock or SPI clock
118	CIO1/SDA/SDI	I/O	I^2C data or SPI data in
119	CIO2/EN_IWPU/SDO	I/O	Enable I^2C internal Weak Pull-Up resistors or SPI data out
120	CI3/EN_ISPU/nSS	I	Enable I^2C internal Strong Pull-up or SPI slave select
121	CIO4/A0/SRDY	I/O	I^2C address bit or SPI data ready
127	CI5/A1/CK_Pol	I	I^2C address bit or SPI SCK Polarity
132	CI6/A2/CK_Pha	I	I^2C address bit or SPI SCK Phase
133	CI7/A3/MSB_First	I	I^2C address bit or SPI MSB First selection
134	CI8/IRQ_Pol	I	IRQ polarity
116	IRQ	O	Interrupt request output (see notes below)
122	CLK	I	External clock (see notes below)
131	FR	I/O	Rows synchronization signal / Test (see notes below)
143, 144, 145, 147, 149, 151, 153, 155	CP1H to CP4H CP1L to CP4L	I/O	External capacitors pads for LCD voltage multiplier
115	RFU2	I	should be left open or connected to VSS
114	RFU1	I	should be left open or connected to VSS

Table 5 Pin description

Note: I: Input O: Output

Notes:
See **section 7** for supply connections and external components

EN: Chip enable, active high. When this signal is low, the device is in Disable mode and regulators are switched off. Power supply is applied to the pads only in standard configuration. At power-up or immediately after power-up, EN must be high and an external reset is recommended.

LSV: If LSV is 1, the low supply voltage configuration (1.2 to 2V) is selected; otherwise the standard configuration (2 to 3.6 V) is selected.

VLCD_IN: LCD voltage input. Must be connected to VLCD_OUT when the internal voltage generation is used (EN_IVLCD=1). In external VLCD mode (EN_IVLCD=0), VLCD_IN must be connected to an external voltage supply (max. 7.6V).

VLCD_OUT: LCD voltage generator output. The internal voltage multiplier must be deactivated (EN_IVLCD=0) when VLCD_OUT is not connected to VLCD_IN (over voltage risk). External 1μF capacitor is required between VLCD_OUT and VSS when the internal VLCD generator is used.

VLED[1:0]: Programmable voltage output for LED. VLED is doubled (2 pads) for better drive capability. VLED should be connected to VDD when the LED driver is not used.

IRQ: Interrupt. This line is active to initiate a communication with the host. If CI8 is low, this line is active low otherwise it is active high.

CLK: External clock input if selected by the appropriate command. If the external clock is not used, this pad should be connected to Ground.

FR: External rows synchronization input if selected by the appropriate command or internal rows synchronization output.

6 FUNCTIONAL DESCRIPTION

6.1 Standard multiplex addressing technique

6.1.1 LCD driver output

Applying a DC voltage to a LCD will cause electro-chemical reactions which shorten the lifetime of the LCD. For this reason, the drive voltage must be alternating.
The frequency of the drive voltage must be at least 30 Hz to prevent display flicker. An upper frequency is set by coupling and relaxation effects which cause ghosting and irregular contrast in the display. The upper frequency limit is approximately 200 Hz. The current consumption increases in direct proportion to the drive frequency.

The voltage across a pixel is:
Vp = Vr – Vc where Vr and Vc are the voltages applied respectively on a row (common) and a column (segment).
The voltage across an off pixel is **Vp < Vth**, where Vth is the LCD threshold voltage and the voltage across an on pixel is **Vp > Vth**.
The row selection voltage is **Vr = S** for the selection time **Δt =T/N**, where T is the frame time and N the number of rows. Outside the selection time, the row is grounded with potential zero. The column (data) voltage is **Vc = (- F)** for an on pixel and **Vc= (+ F)** for an off pixel.
Vp = S + F for an **on pixel** and **Vp = S – F** for an **off pixel**
Vp= (+/- F) during non-addressed states with **|F| < Vth**.
A dc-free addressing could be realized with the addressing voltages Vr and Vc having a reverse sign as shown in the following figure:

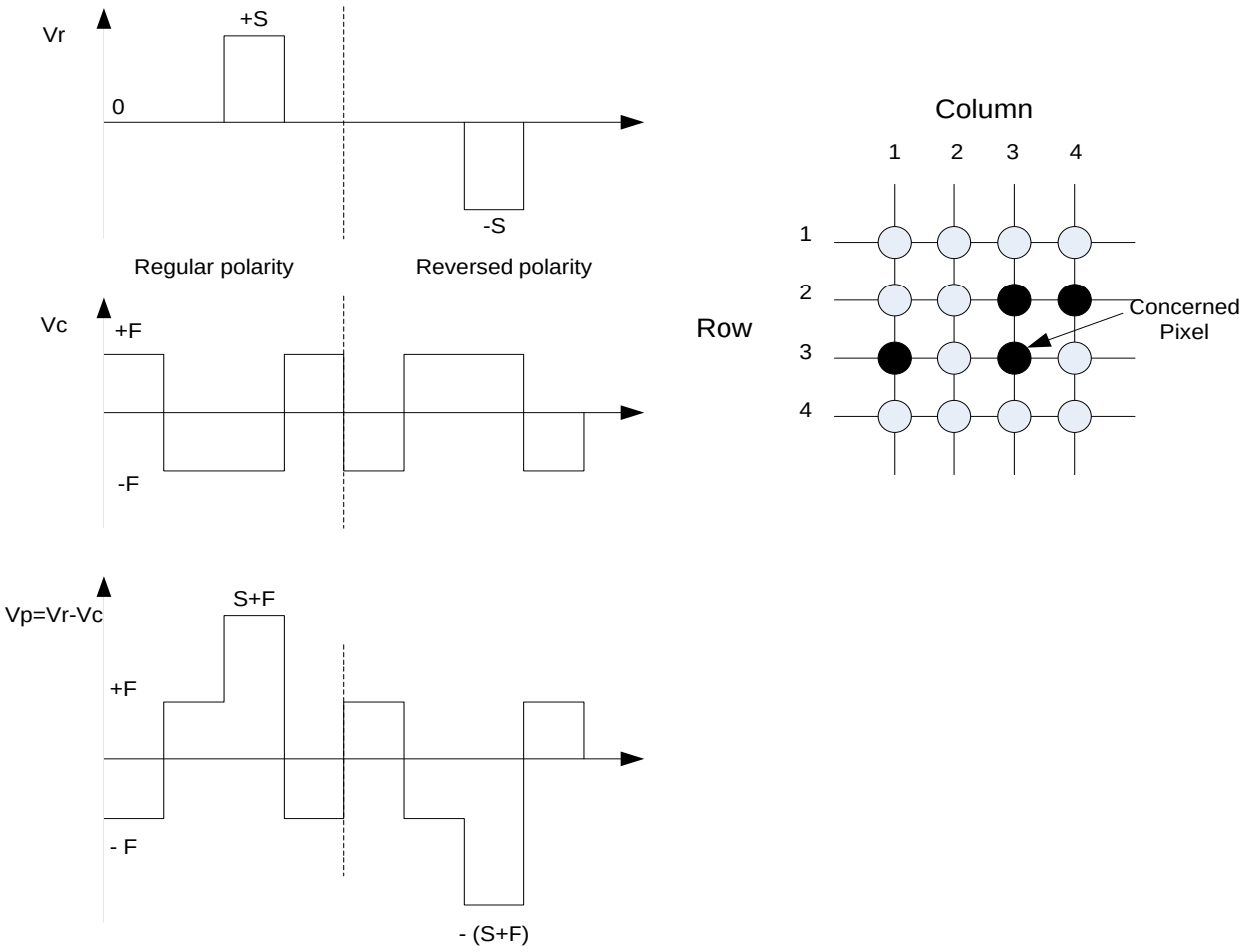


Figure 5 Columns (data) and rows (commons) addressing voltages

The voltage swing of the row (common) drivers is 2S. To reduce this swing, the regular polarity could be offset by F and the reversed polarity by S resulting in the same regular and reversed polarity for the pixel voltage Vp as shown in the following figure:

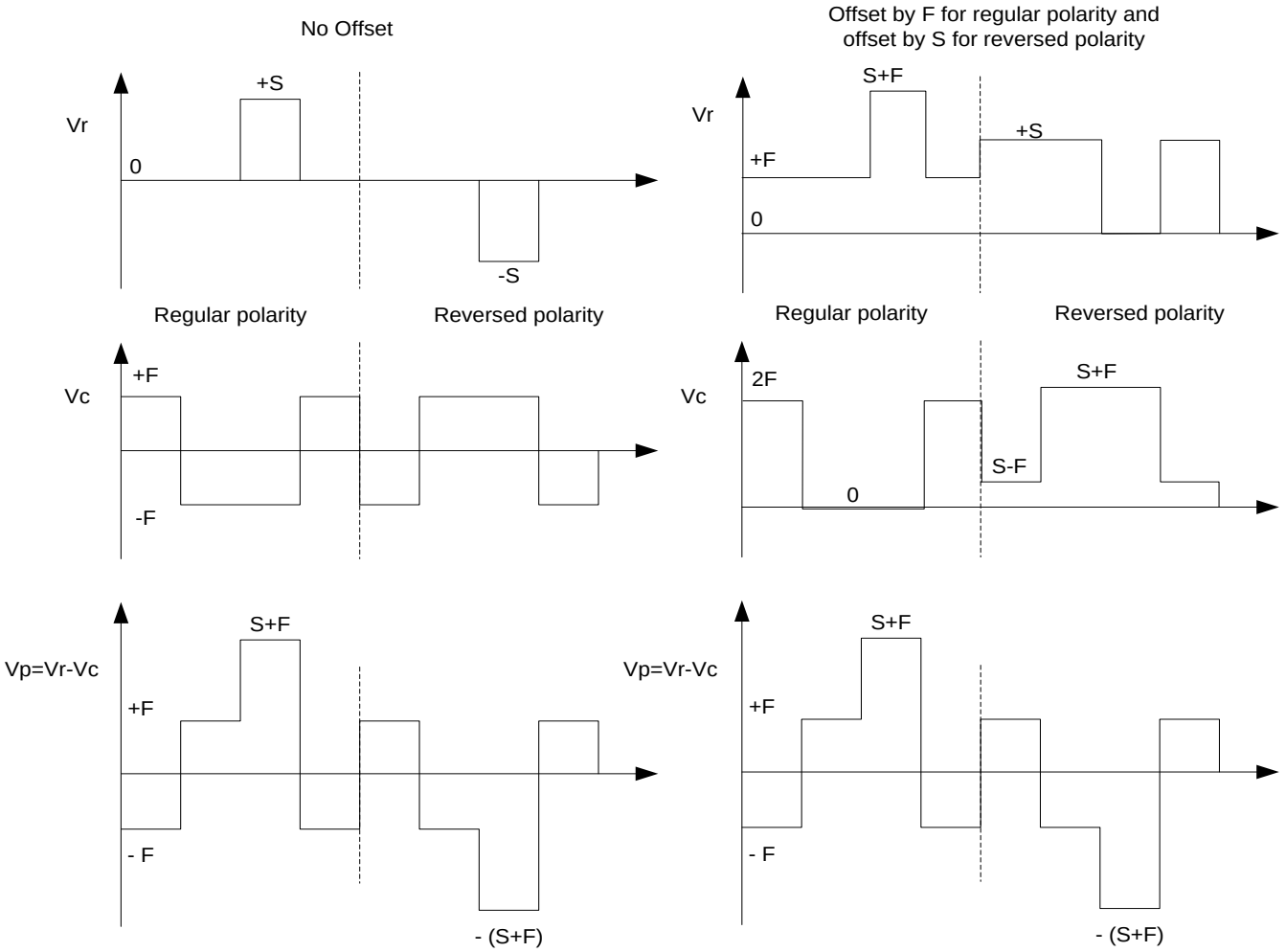


Figure 6 Addressing voltages without and with offset

The required voltages for the column or row drivers are 0, F, 2F, S, S+F and S-F. These voltages can derived from the voltage source S+F with a buffered voltage divider.

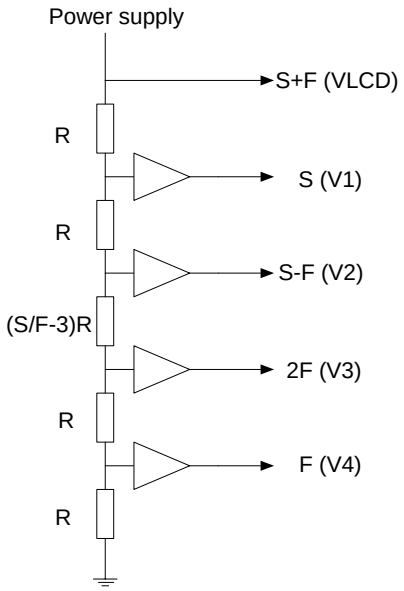


Figure 7 Intermediate voltages generation

With the bias ratio defined as B = F/(S+F), the resistor in the middle assumes the value (1/B-4) R. VLCD is the power supply of the voltage divider (VLCD = S+F).

6.1.2 LCD Supply Voltage generator

In order to use different LCD types, the on-chip generated VLCD is adaptable. A selectable X1, X2, X3, X4 or X5 multiplier is available to generate the VLCD range from the VDD supply voltage. VLCD value can be programmed from 1.25V to 7.6V by 50 mV step. As the LCD threshold voltage is changing with the temperature, VLCD has to change too. Temperature compensation parameters are available to take into account this characteristic.

6.1.3 Bias Voltage generator

Intermediate voltages for LCD display are generated on chip. The optimum levels depend on the multiplex rate and the LCD threshold voltage (Vth). The optical effect produced in the display depends on the RMS value of the drive voltage.
The RMS voltages for an on pixel and off pixel are:

$$\text{Von (RMS)} = \frac{1}{\sqrt{T}}\sqrt{(S+F)^2\frac{T}{N}+F^2\frac{T}{N}(N-1)}$$

$$\text{Voff (RMS)} = \frac{1}{\sqrt{T}}\sqrt{(S-F)^2\frac{T}{N}+F^2\frac{T}{N}(N-1)}$$

The optimum ratio providing the maximum contrast between an on pixel and an off pixel Von/Voff becomes a maximum for S/F = $\sqrt{N}$.

The optimal value for the bias ratio is 1/ ($\sqrt{N}$ + 1) where N is the number of rows.

The following table gives values of VLCD in reference to RMS voltage applied to a pixel off and the contrast achieved between an ON and OFF pixel. The selected bias ratio is the more optimal (depending on the multiplex rate).

Nb. of rows/ Multiplex rate	Selected bias ratio	BR	VLCD/Voff(RMS)	Von (RMS)/ Voff(RMS)	V1/VLCD	V2/VLCD	V3/VLCD	V4/VLCD
32 1: 32 MUX	1/6.5	111	5.136	1.196	0.8461	0.6923	0.3076	0.1538
24 1: 24 MUX	1/6	110	4.707	1.230	0.8333	0.6665	0.3334	0.1666
20 1: 20 MUX	1/5.5	101	4.400	1.255	0.8181	0.6363	0.3636	0.1818
16 1: 16 MUX	1/5	100	4.082	1.291	0.7999	0.5999	0.4000	0.2000
	1/ 4.5	011			0.7777	0.5555	0.4444	0.2222
10 1: 10 MUX	1/4	010	3.508	1.387	0.7499	0.5000	0.5000	0.2500
8 1: 8 MUX	1/4	010	3.411	1.446	0.7499	0.5000	0.5000	0.2500
	1/ 3.5	001			0.7141	0.4286	0.5713	0.2858
4 1: 4 MUX	1/3	000	3.000	1.732	0.6665	0.3334	0.6665	0.3334
3 1: 3 MUX	1/3	000	3.000	1.915	0.6665	0.3334	0.6665	0.3334
2 1: 2 MUX	1/3	000	3.000	2.236	0.6665	0.3334	0.6665	0.3334

Table 6 Bias ratio

We can observe in this table that the partial display mode decreases VLCD, leading to lower power consumption. Current consumption is also decreased because lower VLCD leads to choose fewer stages for voltage multiplier and the efficiency is improved.

6.2 Static Drive Addressing Technique

The static or direct drive is used for one row drive (or common). The row is driven by a square wave having a peak to peak value VLCD. To switch on a pixel (or segment), the inverse of the row must be applied to produce an RMS voltage between the row and the column. To switch off a pixel, the column is driven with the row waveform.

6.3 Active addressing technique

The active addressing technique follows a totally different approach compared to the multiplex addressing technique. The steps are given bellows:

- An N-bit word is chosen as row-select pattern. The row select voltages are chosen to be zero for logic 0 and VLCD for logic 1
- The row-select and the data patterns (columns) are compared bit by bit
- The number of mismatches 'i' between these two patterns is determined by counting the number of exclusive OR high results
- The column voltage is decided by a majority decision. The column is zero if 'i' is less than N/2 and VLCD if 'i' is greater than N/2

These operations are repeated for all the columns.

A cycle is completed when all the 2^N binary patterns are covered as row-select pattern once. The time duration should be small as compared to the response time of the display. The time duration of a cycle (2^N T) should be low in order to avoid flicker in the display. The rms voltage across the pixels is independent of the sequence in which the 2^N row select patterns are chosen for addressing the display. This allows some freedom in the choice of the sequence to suit the display characteristics (the functions used for the rows should only be orthogonal).

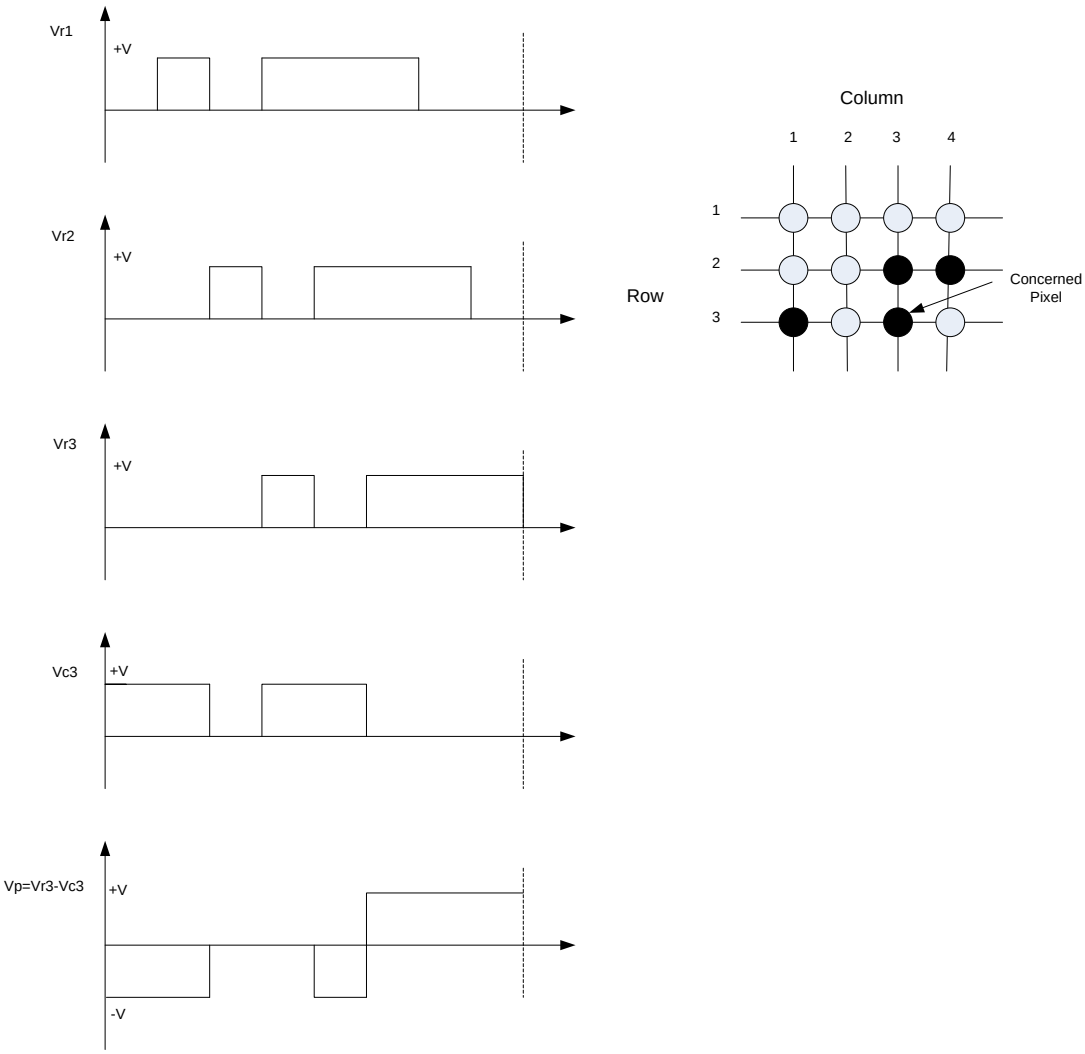


Figure 8 Active addressing waveforms

The advantages of this addressing technique are:

- Simple addressing waveforms with just two level voltages (0 and VLCD)
- Natural DC-free operation
- Low supply voltage

The disadvantages are:

- Not suitable for displays with large rows number N (N should not be greater than 11)
- N must be odd

To use this addressing technique on a 32 row display, identical rows are grouped together
In the EM6127 driver, 9 row groups are used. The VLCD voltage in active addressing is 1.659 x Vth where Vth is the LCD threshold voltage. The LCD and driver consumptions are strongly decreased in this mode.
To use the active addressing technique, the user must:
- select a one character line mode (Mode 0 or 14) with the command Select Mode *(43h)*,
- change the VLCD level (*5Ah-5Bh)*
- set the bit ACTADR to 1 with the command Display Control *(41h)*

An x2 or x3 zoom function may be used to double or triple the size of the 5x7 character. The corresponding bits are in the Select Mode command.
If the text does not change and the functions (blink, sequence, scrolling) are not used, it is possible to decrease this consumption by decreasing the oscillator frequency from 576 kHz to 54 kHz with the command Driver/Pads configuration. The active addressing single pulse duration should be lower than the LCD response time to avoid flickering.

(5Eh) and Timing control (5Dh).

6.4 LED driver

EM6127 contains a driver for two LEDs for back or front light illumination. LED light on LCD modules can be driven with a DC voltage through an external current limiting resistor. When the primary consideration is bright display with the lowest possible power consumption, pulse width modulation (PWM) has several advantages. If instead of a constant value, the current is applied a part of the time, the power consumption is reduced and the seen result is the same because the human eye has a certain amount of persistence. If exposed to a bright light, the eye will remember the light for a short period of time. The pulse repetition frequency is greater than 100 Hz so the flickering is not perceptible to the eye.
PWM duty cycle is programmable to drive different types of LED. The connection should be as follows:

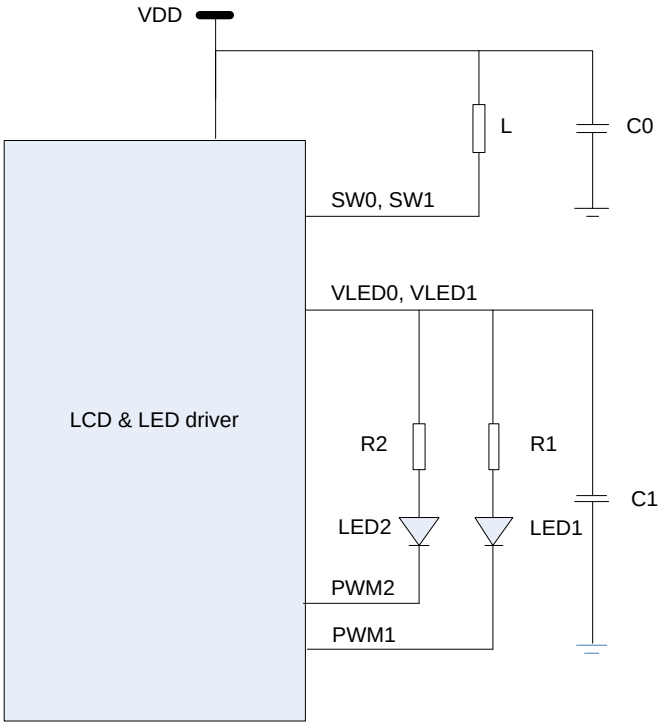


Figure 9 LED connection

The recommended values are 50 uH for L and 10 uF for C0 and C1. The R1 and R2 values depend on programmed VLED and the type of LED. If the internal voltage generator is not used, the coil can be removed.
Pads SW, VLED are each doubled for better drive capability.

6.5 Oscillator

For the full display mode, the frequency Fref of the reference oscillator is 7680 time the frame frequency (ie Fref = 576 kHz for a frame rate of 75Hz). In one character line mode, the oscillator frequency can be reduced until 54 kHz to decrease power consumption.
An external clock signal can be used by setting the corresponding bit in the Timing Control command (see 0).

6.6 Power on reset

The power-on-reset block initializes the chip after a power on or a power failure.

6.7 Memories Map

The EM6127 chip contains a RAM of 1536 words (16 bits) and a ROM of 8192 words (16 bits). The memory map is as follows:

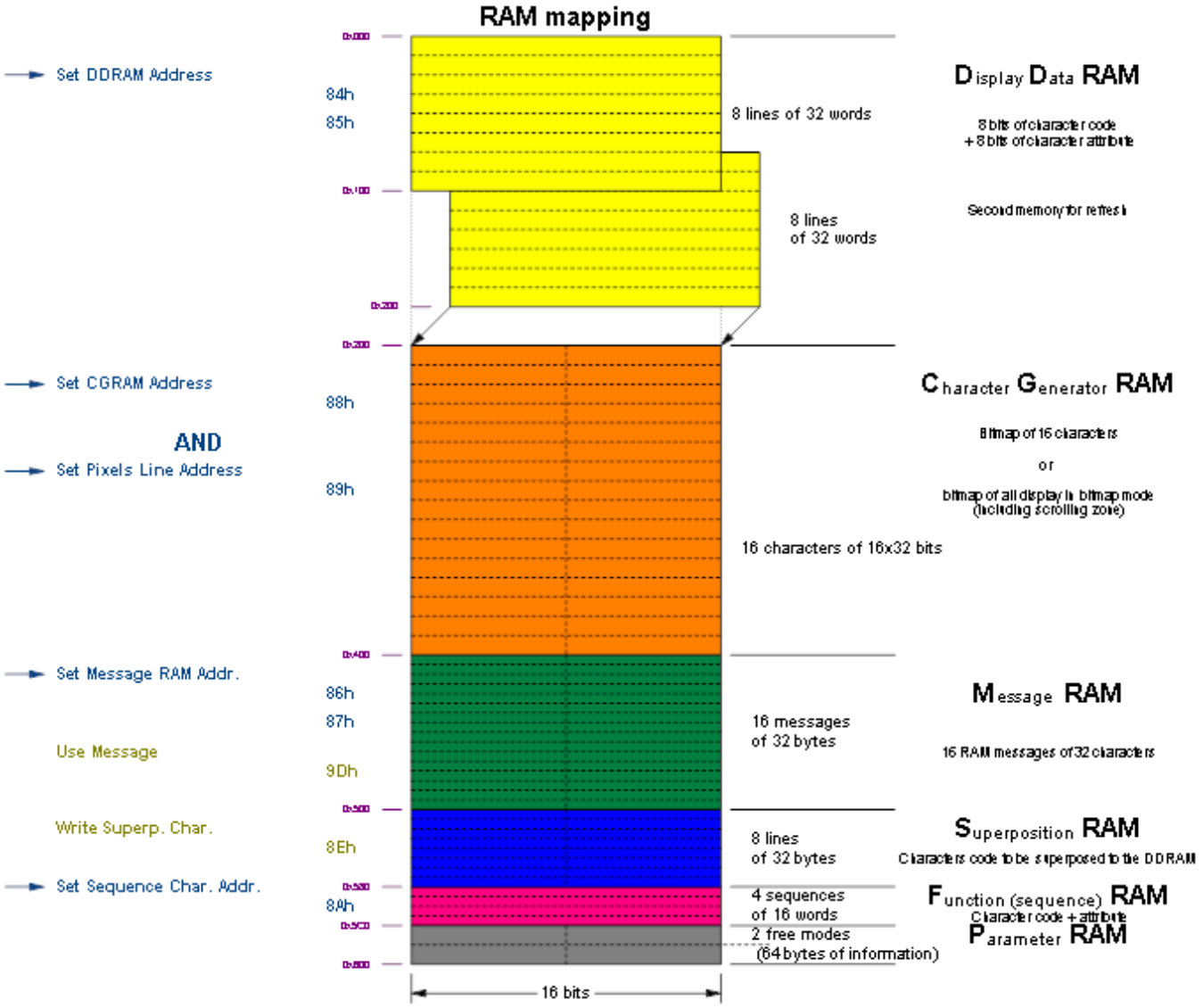


Figure 10 RAM Mapping

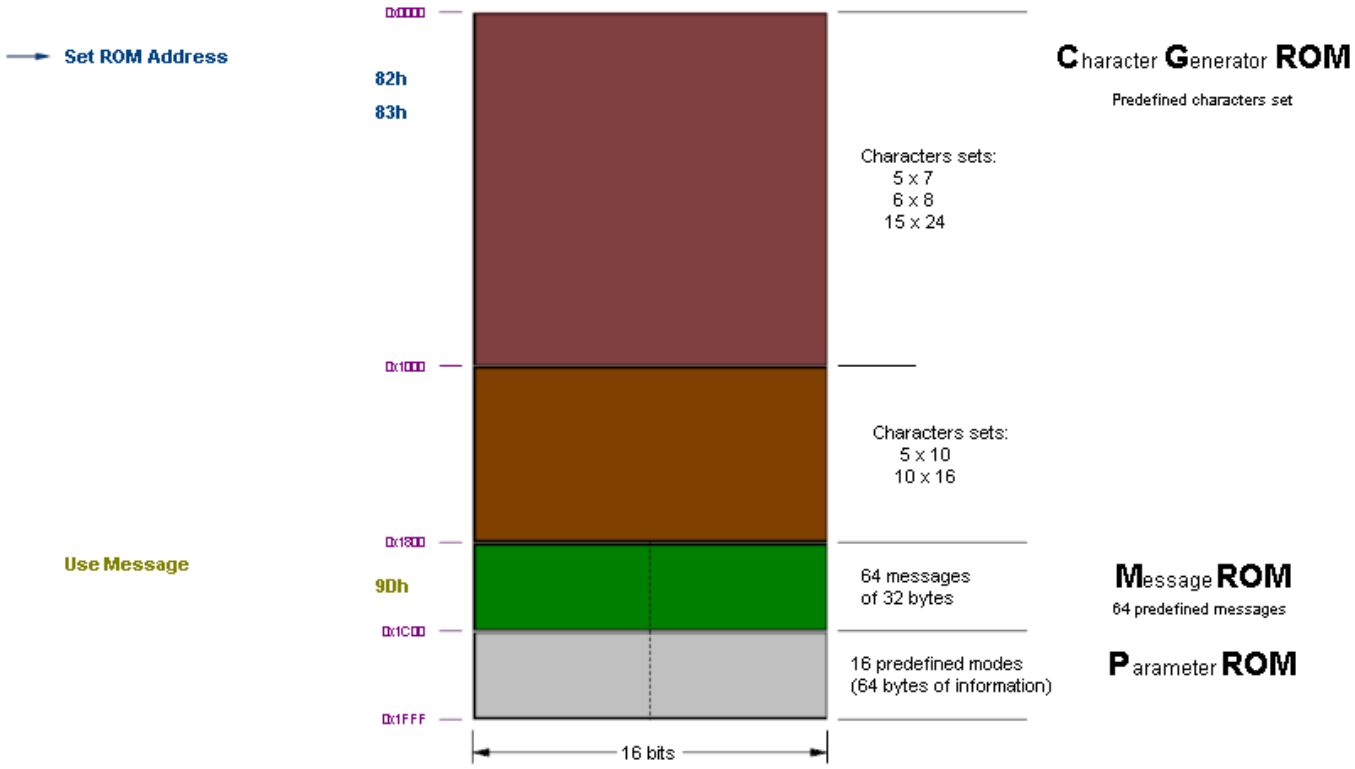


Figure 11 ROM Mapping

6.8 DDRAM

EM6127 contains a DDRAM (Display Data RAM) which stores the address of the character defined in the CGROM or CGRAM. The DDRAM stores 8x32 words. Each word contains a byte of special-function or character-control bits (see commands 98h-99h-9Ah, *picture/character control*), followed by an ASCII code. The DDRAM represents a virtual canvas of 32 columns by 8 rows. Depending on the display mode and scrolling state, a subset of this virtual canvas will appear on the display. The 3 MSB bits of the DDRAM address contains the line number. The 5 LSB bits gives the character number of a line. The DDRAM has a non-displayed part. The addresses stored in the DDRAM between 00h and 0Fh corresponds to a CGRAM character and the other addresses are for CGROM.

6.9 CGROM

This memory is used for pre-defined characters. 5x7, 6x8, 5x10, 10x16 and 15x24 formats are available. The basic tables contain 112 ASCII characters. Extensions are possible for the remaining 128 characters by using a customer-specific mask. The extensions follow the ISO 8859 Unicode standards and are language dependent. The following table gives the correspondence between ISO 8859 standards and languages.

Norm	Language
ISO 8859-1	Latin-1 or Occidental European
ISO 8859-2	Latin-2 or Central European
ISO 8859-3	Latin-3 or South European
ISO 8859-4	Latin-4 or North European
ISO 8859-5	Cyrillic
ISO 8859-6	Arab
ISO 8859-7	Greek
ISO 8859-8	Hebrew
ISO 8859-9	Latin-5 or Turkish
ISO 8859-10	Latin-6 or Nordic
ISO 8859-11	Thai
ISO 8859-12	-
ISO 8859-13	Latin-7 or Baltic
ISO 8859-14	Latin-8 or Celtic
ISO 8859-15	Latin-9
ISO 8859-16	Latin-10 or South-East European

Table 7 ISO 8859 norms

Contact EM for languages requiring more than 128 special characters and not represented in the above table.

The basic table is coded as follows:

Figure 12 CGROM contents (5x7 characters format)

The tables for the other characters formats are shown in the annexes. If the ROM extension is used, the mapping will follow the same principle. Address 80h to 8Fh will use the CGRAM characters (the same characters as the address 00h to 0Fh). CGROM characters will start at address 90h.

6.10 CGRAM

Up to 16 user-defined characters of maximal dimension 16x32 may be stored in the character generator RAM.

6.11 Messages Memories

Additional ROM and RAM memory spaces are included in the chip for messages. 64 messages of up to 32 characters are stored in ROM and 16 application-specific messages of up to 32 characters can be programmed in RAM.

6.12 Superposition RAM

This RAM part contains characters code to be superposed with the characters in the DDRAM. This feature is used for language with accents.

6.13 Sequence RAM

The chip contains 4 sequences of 16 characters with attributes. Only blank, blink, inverse, inverse blink and cursor are possible on a sequence character.

6.14 Parameters memories

16 predefined modes in ROM and 2 free modes in RAM are available. The parameters memories contain display and character lines data: display rows, columns number, line start (row and column), characters format, cursor format and spaces.

6.15 EEPROM

An EEPROM is included in the chip to store trimming values, communication parameters. This EEPROM can also contain default LCD configurations:

- LCD on or off
- LCD Mode
- Active addressing enable or disable
- 4 predefined messages with attributes
- VLCD level

The EEPROM is read at reset.

6.16 Shift Register

The shift register contains data to be displayed of one LCD pixels row.

6.17 Interface

Two different serial interfaces are available. The EM6127 chip is always a slave whatever interface is selected.
The I^2C compatible interface is a two wires interface (serial clock and serial data). The serial clock (SCL) provides the timing for the interface. The serial data (SDA) is a bidirectional and is used to transfer data.
The serial peripheral interface (SPI) is a five wire interface (Chip Select, Slave Ready, Clock, Data in and Data out). When the Chip Select (nSS) is high, the chip is deselected and the data out (SDO), the Slave Ready signal (SRDY) are held in high impedance state. The clock (SCK) provides the timing for the serial interface.
For both interfaces, the data are 8 bits oriented.

6.17.1 Protocol

Data and commands must be exchanged with the LCD driver. A transfer begins always with a command. When the command is Write Data, the bytes following the command are data until the transfer is stopped (STOP condition with I2C interface or nSS driven high for SPI).

6.17.2 Configuration

The interface is selected through the CIS signal. If CIS is low, the SPI interface is selected. If CIS is high, the I2C interface is used. Pads are configured as follows:

Pads	CIS=0			CIS=1		
	Name	**Description**	**Type**	**Name**	**Description**	**Type**
CIO0	SCK	SPI Clock	Input	SCL	I2C clock	Input/Output
CIO1	SDI	SPI data in	Input	SDA	I2C data	Input/Output
CIO2	SDO	SPI data out	Output	EN_IWPU	Enable I2C internal weak pull-up resistors on CI0, CI1	Input
CI3	nSS	SPI slave select	Input	EN_ISPU	Enable I2C internal strong pull-up resistors on CI0, CI1	Input
CIO4	SRDY	SPI data ready	Output	A0	I2C address bit	Input
CI5	CK_Pol	SPI clk polarity	Input	A1	I2C address bit	Input
CI6	CK_Pha	SPI clk phase	Input	A2	I2C address bit	Input
CI7	MSB_First	SPI MSB First	Input	A3	I2C address bit	Input
CI8	IRQ_Pol	IRQ Polarity	Input	IRQ_Pol	IRQ Polarity	Input

Table 8 Pads configuration

Notes: If CI8 is low, IRQ is active low, otherwise high.
The weak and the strong pull-up resistors have the respectively values 40 kOhms and 20 kOhms.

6.17.3 I2C interface

EM6127 has a slave only I²C interface. Both data and clock lines remain high when the bus is not busy. A high to low transition of the data line, while the clock is high is defined as a START condition. A low to high transition of the data line while the clock is high is defined as a STOP condition. One data bit is transferred during each SCL pulse. The data on SDA line must remain stable during the high period of SCL pulses, as any changes at this time would be interpreted as START or STOP condition. Data is always transferred with MSB first.

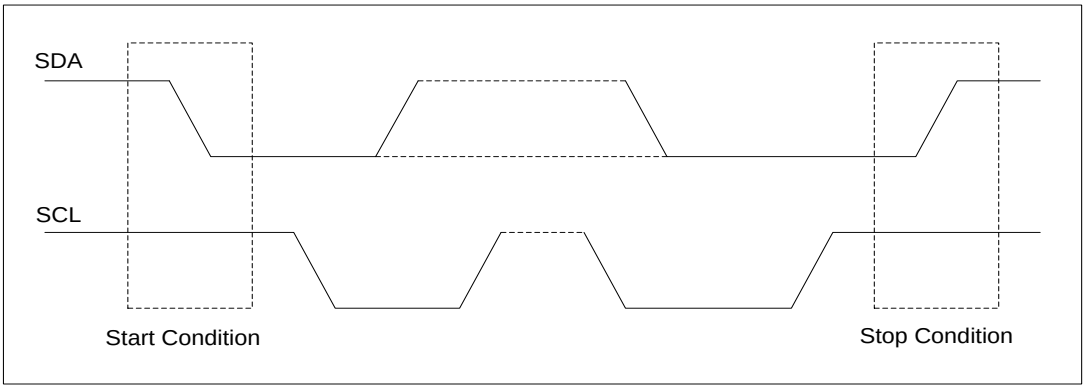


Figure 13 I²C Start and Stop condition

The number of data bytes between the START and STOP condition is unlimited. Each byte of eight bits is followed by an acknowledge bit.
After a START condition, the slave address combined with R/W bit must be sent first. If the slave address corresponds to the EM6127 slave address, it will send an acknowledge bit by pulling down the SDA line and the data transfer is enabled.
EM6127 LCD driver has the slave address coded on 7 bits: 0010000 (This address is also called Device address). The 4 LSB bit of the address are configurable by setting the signals A[3..0].
The I²C bus configurations for the read and write operations are shown in the following figures:

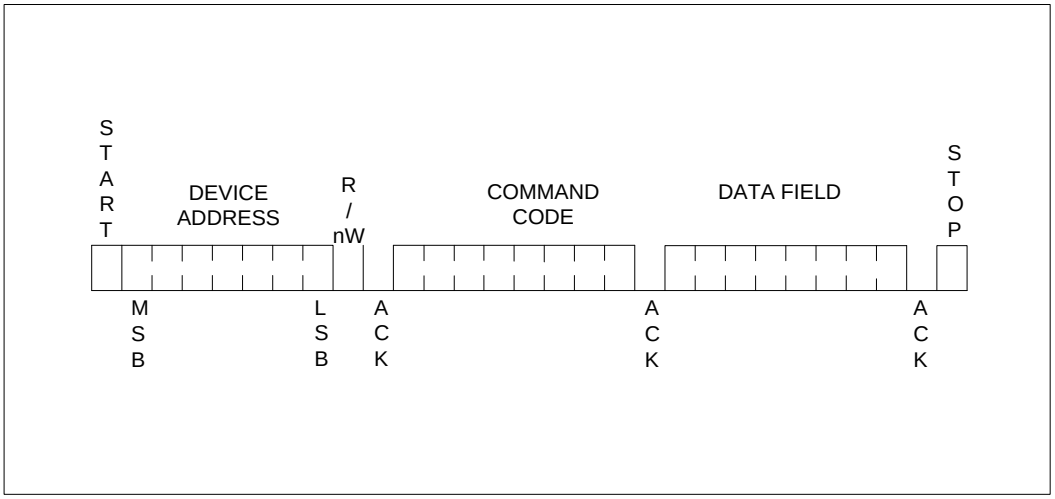


Figure 14 Command sending

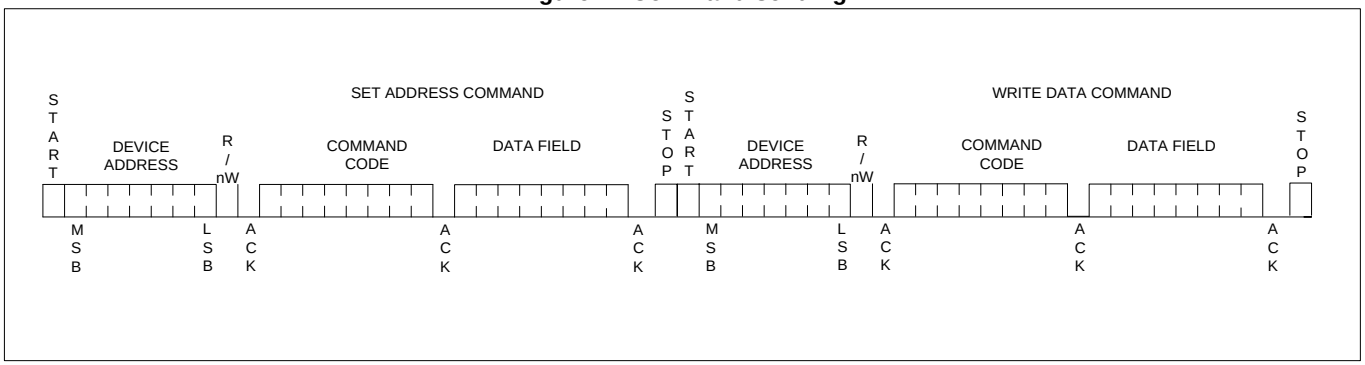


Figure 15 Setting address and Writing Data

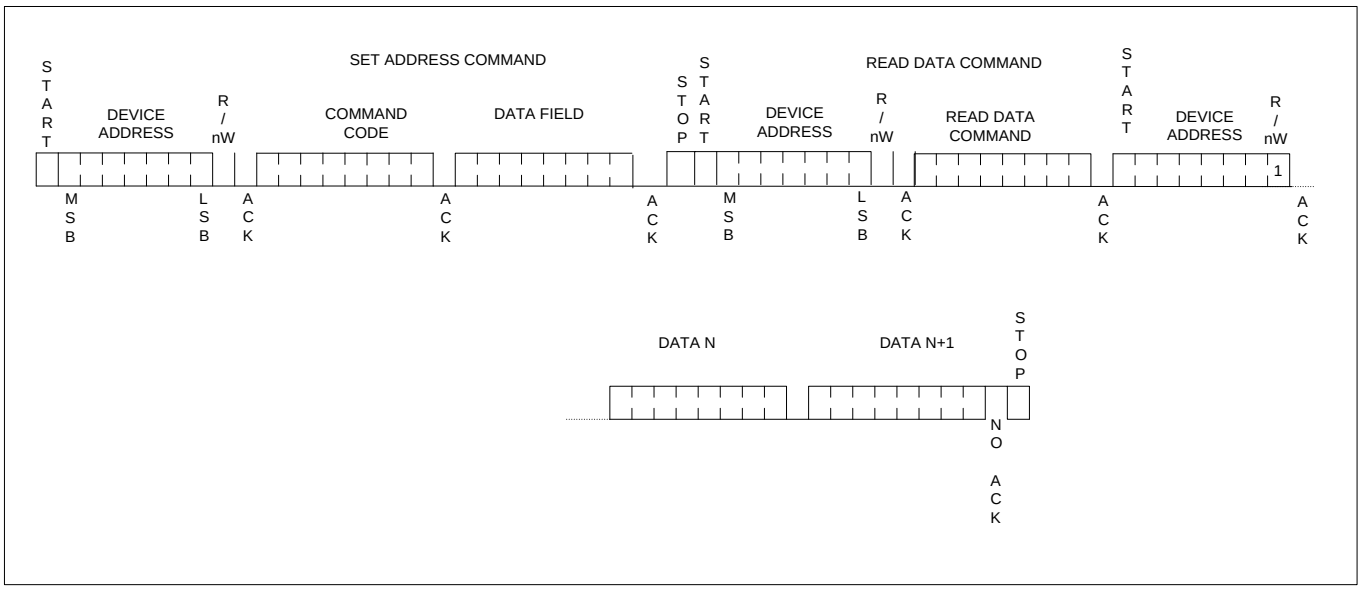


Figure 16 Setting Address and Reading Data

6.17.4 SPI interface

The SPI interface is slave only. Data transfer starts with a command byte. After setting the nSS to low, the host has to wait that the SRDY signal goes to high before sending clocks. At the end of an SPI command, the host must also wait for the SRDY high level before sending data again. The SRDY low duration can vary depending on operations initiated by the SPI command.
Before setting nSS to back to high, the host has to wait again that the SRDY signal goes to high.
During write operations, dummy data are sent on SDO line.
Three signals allow the configuration of the SPI.
If the MSB_First signal is 1, all bytes are sent with the MSB first.
The signal CK_Pol selects polarity of clock and the signal CK_Pha set the edge of data sampling as follows:

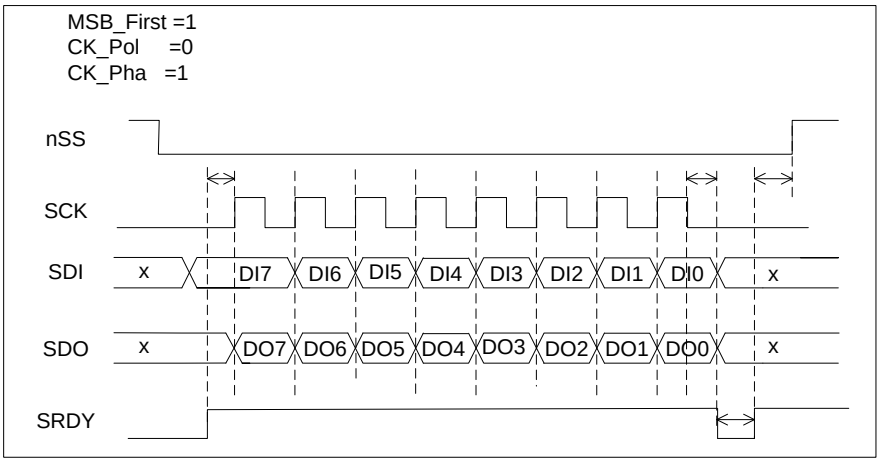


Figure 17 SPI timing with MSB_First=1, CK_Pol=0, CK_Pha=1 (SDO and SRDY are Hi-Z when NSS = 1)

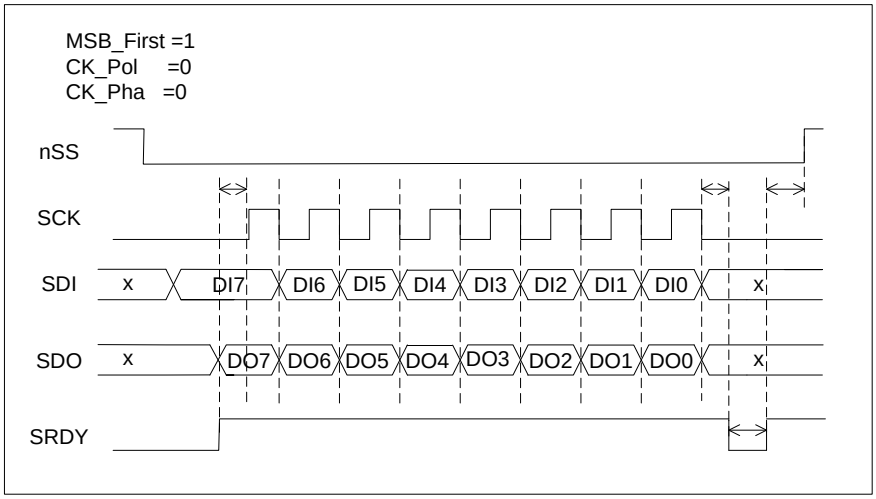


Figure 18 SPI timing with MSB_First=1, CK_Pol=0, CK_Pha=0 (SDO and SRDY are Hi-Z when NSS = 1)

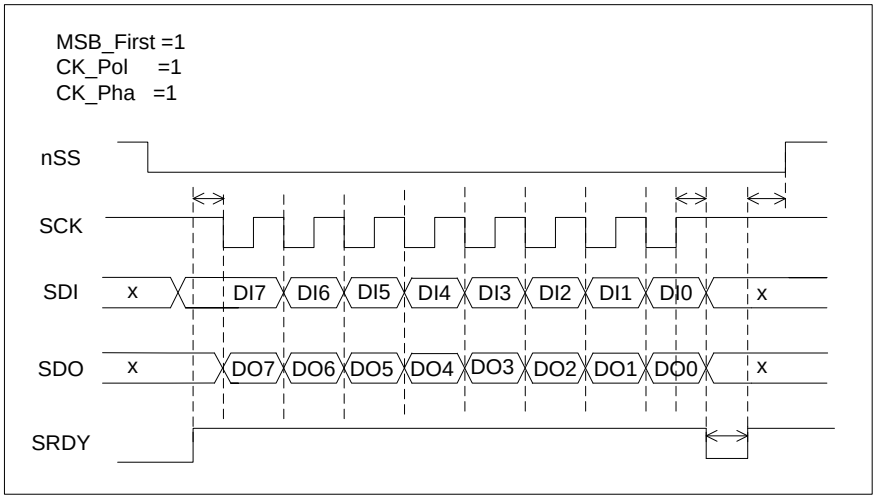


Figure 19 SPI timing with MSB_First=1, CK_Pol=1, CK_Pha=1 (SDO and SRDY are Hi-Z when NSS = 1)

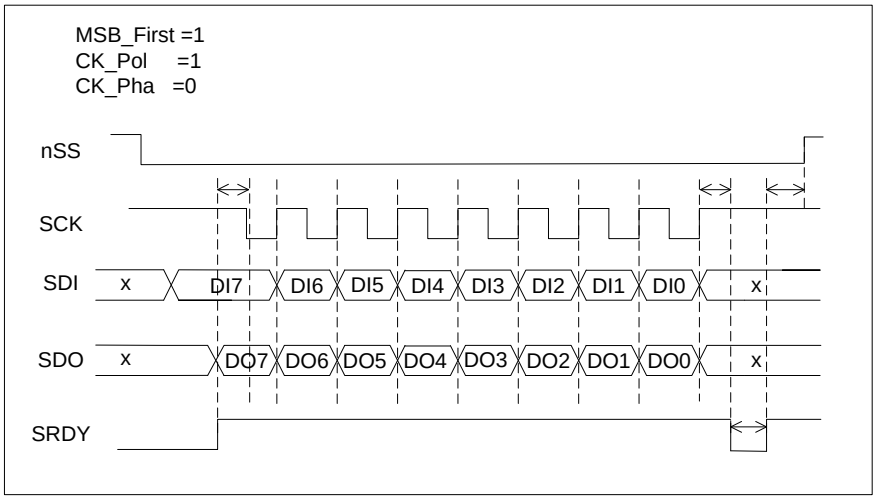


Figure 20 SPI timing with MSB_First=1, CK_Pol=1, CK_Pha=0(SDO and SRDY are Hi-Z when NSS = 1)

The SPI configurations for the read and write operations are shown in the following figure:

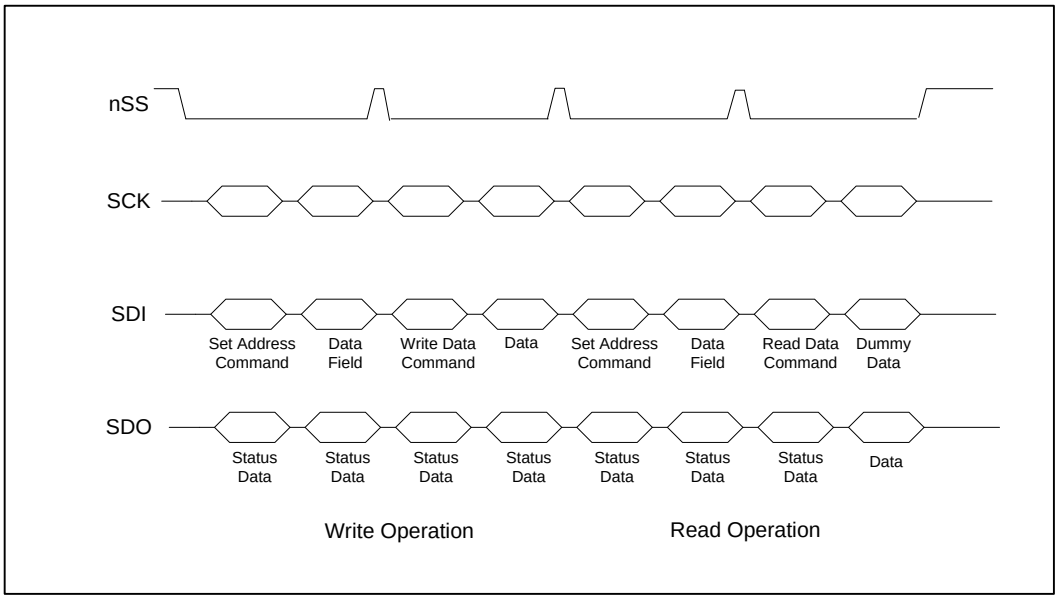


Figure 21 SPI write and read with setting Address

6.17.5 Commands List

The commands are defined in the following table:

Command	Code (8 bits)	Data field	D7	D6	D5	D4	D3	D2	D1	D0
Sleep	01h	No	-	-	-	-	-	-	-	-
Refresh Display	02h	No	-	-	-	-	-	-	-	-
Return Home	03h	No	-	-	-	-	-	-	-	-
Clear Display	04h	No	-	-	-	-	-	-	-	-
Auto Display	05h	No	-	-	-	-	-	-	-	-
Display Control	41h	Yes	ACTADR	FEXCLK	AR	RR	RC	I	BI	ON
LED Control	42h	Yes	LEDINTV	LEN	L2DC2	L2DC1	L2DC0	L1DC2	L1DC1	L1DC0
Select Mode	43h	Yes	CHB	ZO1	ZO0	FM_EN	M3	M2	M1	M0
Cursor Control	44h	Yes	CSP	CFA	BFA	D/I	AU_RD	AU_WR	CIB	CB
Cursor Char Def.	45h	Yes	CCH7	CCH6	CCH5	CCH4	CCH3	CCH2	CCH1	CCH0
Blink Control	46h	Yes	BN2	BN1	BN0	BDC1	BDC0	BF1	BF0	BST
Scrolling Config.	47h	Yes	SWCTRL	SF2	SF1	SF0	R/L	D/U	CONTX	CONTY
Scrolling Nb. Control (1)	48h	Yes	SHN7	SHN6	SHN5	SHN4	SHN3	SHN2	SHN1	SHN0
Scrolling Nb. Control (2)	49h	Yes	SVN7	SVN6	SVN5	SVN4	SVN3	SVN2	SVN1	SVN0
Scrolling Nb. Control (3)	4Ah	Yes	SVN11	SVN10	SVN9	SVN8	SHN11	SHN10	SVN10	SHN8
Scrolling Max. Control (1)	4Bh	Yes	MXH7	MXH 6	MXH 5	MXH 4	MXH 3	MXH 2	MXH 1	MXH 0
Scrolling Max. Control (2)	4Ch	Yes	-	-	-	-	-	-	MXH9	MXH8
Scrolling Max. Control (3)	4Dh	Yes	MXV7	MXV6	MXV5	MXV4	MXV3	MXV2	MXV1	MXV0
Char Scrolling disable(1)	4Eh	Yes	SCH17	SCH16	SCH15	SCH14	SCH13	SCH12	SCH11	SCH10
Char Scrolling disable (2)	4Fh	Yes	SCH9	SCH8	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2
Char Scrolling disable (3)	50h	Yes	SCH1	SCH0	-	-	-	-	-	-
Line Scrolling disable (1)	51h	Yes	SL31	SL30	SL29	SL28	SL27	SL26	SL25	SL24
Line Scrolling disable (2)	52h	Yes	SL23	SL22	SL21	SL20	SL19	SL18	SL17	SL16
Line Scrolling disable (3)	53h	Yes	SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8
Line Scrolling Disable(4)	54h	Yes	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0
Init Sequence	55h	Yes	SEQRS	SEQF1	SEQF0	SEQRU4	SEQRU3	SEQRU2	SEQRU1	SEQONCE
Blank Line	56h	Yes	BLA8	BLA7	BLA6	BLA5	BLA4	BLA3	BLA2	BLA 1
Blink Line	57h	Yes	BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1
Invert Line	58h	Yes	IL8	IL 7	IL 6	IL 5	IL 4	IL 3	IL 2	IL 1
Interrupt Mask	59h	Yes	WDOGM	LCDERRORM	BPROM	BDCM	ESCRXM	ESCRYM	ESEQM	EBLM
VLCD and Bias Control (1)	5Ah	Yes	EN_IVLCD	VL6	VL5	VL4	VL3	VL2	VL1	VL0
VLCD and Bias Control (2)	5Bh	Yes	TC1	TC0	REDUC	VMU1	VMU0	BR2	BR1	BR0
VLED Control	5Ch	Yes	-	CK_LD1	CK_LD0	VLD4	VLD3	VLD2	VLD1	VLD0

Command	Code (8 bits)	Data field	D7	D6	D5	D4	D3	D2	D1	D0
Timing Control	5Dh	Yes	EFR	ECK	CK_VRF	CF1	CF0	FR2	FR1	FR0
Driver/Pads Configuration	5Eh	Yes	ADIV_ SEL	AOSC_ SEL	ADIS_ RD	AVREF_ SEL	DIS_ WDOG	DIS_FR_ P/U	EN_FR_ OUT	IRQ_PP
Display Mask	5Fh	Yes	-	L_ST2	L_ST1	L_ST0	-	L_END2	L_END1	L_END0
Set Display Rows Nb.	6Fh	Yes	MUX1LP	MUX1DR	RN5	RN4	RN3	RN2	RN1	RN0
Set Line Start Column	70h	Yes	-	X6	X5	X4	X3	X2	X1	X0
Set Line Start Row	71h	Yes	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Select Character Set (1)	72h	Yes	CHN4	CHN3	CHN2	CHN1	CHN0	CS2	CS1	CS0
Select Character Set (2)	73h	Yes	CAR2	CAR1	CAR0	CBR2	CBR1	CBR0	CH1	CH0
Set Bitmap Width	74h	Yes	ZX1	ZX0	BW5	BW4	BW3	BW2	BW1	BW0
Set Bitmap Height	75h	Yes	ZY1	ZY0	BH5	BH4	BH3	BH2	BH1	BH0
Interrupt Clear	80h	Yes	WDOGB	LCDERR ORB	BPROB	BDCB	ESCRXB	ESCRYB	ESEQB	EBLB
Set Register Address	81h	Yes	-	-	-	RA4	RA3	RA2	RA1	RA0
Set ROM Address (1)	82h	Yes	-	-	-	ROA12	ROA11	ROA10	ROA9	ROA8
Set ROM Address (2)	83h	Yes	ROA7	ROA6	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0
Set DDRAM address(1)	84h	Yes	-	-	-	-	RA3	RA2	RA1	RA0
Set DDRAM address(2)	85h	Yes	-	-	-	CA4	CA3	CA2	CA1	CA0
Set Messages RAM Address(1)	86h	Yes	-	-	-	-	MEA3	MEA2	MEA1	MEA0
Set Messages RAM Address (2)	87h	Yes	-	-	-	CH4	CH3	CH2	CH1	CH0
Set CGRAM address	88h	Yes	-	-	-	-	A3	A2	A1	A0
Set Pixels Line Address	89h	Yes	-	-	-	PL4	PL3	PL2	PL1	PL0
Set Sequence Character address	8Ah	Yes	-	-	S1	S0	N3	N2	N1	N0
Configure Mode and Line	8Ch	Yes	-	-	-	FMN	-	L2	L1	L0
Move Cursor	8Dh	Yes	-	FL	NL	PL	-	CR	MF	MB
Write Superposition Character	8Eh	Yes	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Write Data	8Fh	No	-	-	-	-	-	-	-	-
Blank Complete Line	91h	Yes	BLACL8	BLACL7	BLACL6	BLACL5	BLACL4	BLACL3	BLACL2	BLACL1
Blink Complete Line	92h	Yes	BCL8	BCL7	BCL6	BCL5	BCL4	BCL3	BCL2	BCL1
Invert Complete Line	94h	Yes	ICL8	ICL7	ICL6	ICL5	ICL4	ICL 3	ICL 2	ICL 1
Clear Char. Control	98h	Yes	SEQ	M	SP	C	INB	I	B	BLA
Set Char. Control	99h	Yes	SEQ	M	SP	C	INB	I	B	BLA
Modify Char. Control	9Ah	Yes	SEQ	M	SP	C	INB	I	B	BLA
Scrolling Control	9Ch	Yes	-	-	SCXST	SCYST	SCXSTP	SCYSTP	SCXRS	SCYRS
Use Message	9Dh	Yes	SPM	ME6	ME5	ME4	ME3	ME2	ME1	ME0
Use Sequence	9Eh	Yes	-	-	M3	M2	M1	M0	S1	S0

Command	Code (8 bits)	Data field	D7	D6	D5	D4	D3	D2	D1	D0
Get Interrupt Status	9Fh	No	-	-	-	-	-	-	-	-
Read Superposition Character	AEh	Yes	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Read Data	AFh	No	-	-	-	-	-	-	-	-
Write expanded Data	CFh	No	-	-	-	-	-	-	-	-
Read expanded Data	EFh	No	-	-	-	-	-	-	-	-

Table 9 Commands list

To send less data, the following commands can be combined:

- Blank Complete Line, Blink Complete Line, Invert Complete Line (for example, if the user wishes to blink and invert a line, he has to send the code 96h and the line)
- Set ROM address 1 and Set Rom address 2 (to set a ROM address, the user can send set ROM address 1, ROM address 1 and ROM address 2)
- Set DDRAM address 1 and Set DDRAM address 2
- Set Message RAM address 1 and Set Message RAM address 2
- Set CGRAM address and Set Pixels Line address

Commands code 60h to 6Eh, 76h to 7Fh are reserved and should not be used. For the other non-specified commands, the driver will do nothing or send bad command after the command, one data or two data.

Bits	Description	State after Reset
Display Control *(41h)*		
ACTADR	Active addressing enable	0
FEXCLK	External clock for function	0
AR	Automatic refresh	1
RR	Reverse rows	0
RC	Reverse columns	0
I	Inverse mode	0
BI	Bitmap mode	0
ON	Display on	0
LED Control *(42h)*		
LEDINTV	LED Internal voltage generation enable	0
LEN	LED Enable	0
L2DC[2:0]	LED 2 duty cycle	0
L1DC[2:0]	LED 1 duty cycle	0
Select Mode*(43h)*		
CHB	Checker board test mode	0
ZO[1:0]	zoom	0h
FM_EN	Free mode enable	0
M[3:0]	modes	0h
Use Message *(9Dh)*		
SPM	Superposed message bit	0
ME[6:0]	Message number	0h
Set Display Rows Number (Free Mode) *(6Fh)*		
MUX1DR	Static addressing disable read	0
MUX1LP	Static addressing low power mode	0
RN[5:0]	Rows number	20h
Configure Mode and Line (Free Mode) *(8Ch)*		
FMN	Free Mode number	0
L[2:0]	Characters (or picture) line	0
Set Line Start Column (Free Mode) *(70h)*		
X[6:0]	Line Start column	0
Set Line Start Row (Free Mode) *(71h)*		
Y[7:0]	Line Start row	0
Select Character Set (Free Mode) *(72h-73h)*		
CHN[4:0]	Characters number	0
CS[2:0]	Character set	0
CAR[2:0]	Rows Number after cursor	0
CBR[2:0]	Rows number between cursor and character	0
CH[1:0]	Cursor Height	0
Set Bitmap Width (Free Mode) *(74h)*		
ZX[1:0]	Space before character	0
BW[5:0]	Picture or character bitmap width	0
Set Bitmap Height (Free Mode) *(75h)*		
ZY[1:0]	Space before character	
BH[5:0]	Picture or character bitmap height	0
Blank Complete Line *(91h)*		
BLACL[8:1]	Blank Line number	0
Blink Complete Line *(92h)*		
BCL[8:1]	Blinking line number	0
Invert Complete Line *(94h)*		
ICL[8:1]	Line number to invert	0
Blank Line *(56h)*		
BLA[8:1]	Blank Line number	0
Blink Line *(57h)*		
BL8:1]	Blink line number	0
Invert Line *(58h)*		
IL[8:1]	Invert line number	0
Picture or Character Control Command - Clear*(98h)****, Set****(99h)****, Modify****(9Ah)*		
SP	Character superposition enable	0
INB	Character/Character inverse blink	0
SEQ	Sequence enable	0
C	Cursor display	0

I	Character inverse mode	0
B	Character blink	
BLA	Character blank	0
Write Superposition character *(8Eh)*		
SP[7:0]	Character to superpose	0
Read Superposition character *(AEh)*		
SP[7:0]	Character superposed	0
Cursor Control *(44h)*		
D/I	Cursor and DDRAM Address counter increments or decrements after a character has been written or read	0
AU_RD	Automatic increment or decrement enable for read	1
AU_WR	Automatic increment or decrement enable for write	1
CIB	Cursor blinks when character does not blink (if B is set)	0
CB	Cursor blinks when character blinks (if B is set)	0
Move Cursor *(8Dh)*		
FL	Cursor and DDRAM address counter are set at the first line	0
NL	Cursor and DDRAM address counter are set on the next line	0
PL	Cursor and DDRAM address counter are set on the previous line	0
CR	Cursor and DDRAM address counter are set at the beginning of the line	0
MB	Cursor and DDRAM address counter are set on the previous character	0
MF	Cursor and DDRAM address counter are set on the next character	0
Blink Control *(46h)*		
BN[2:0]	Blink number	0
BDC[1:0]	Blink duty cycle	0
BF[1:0]	Blink Frequency	0
BST	Blink Start	0
Scrolling Control *(9Ch)*		
SCXST	Scrolling horizontal once start	0
SCYST	Scrolling vertical once start	0
SCXSTP	Scrolling horizontal once stop	0
SCYSTP	Scrolling vertical once stop	0
SCXRS	Scrolling horizontal pointer reset	0
SCYRS	Scrolling vertical pointer reset	0
Scrolling Config *(47h)*		
SWCTRL	Software control	0
SF[2:0]	Scrolling Frequency	0
R/L	Right/Left configuration	0
D/U	Down/up configuration	0
CONTY	Continuous scrolling vertical	0
CONTX	Continuous scrolling horizontal	0
Scrolling Nb. Control *(48h-49h-4Ah)*		
SHN[11:0]	Number of pixels to be scrolled in horizontal mode	0FFh
SVN[11:0]	Number of pixels to be scrolled in vertical mode	0FFh
Scrolling Max. Control *(4Bh-4Ch-4Dh)*		
MXH[9:0]	Maximum scrolling pixels in horizontal mode	FFh
MXV[7:0]	Maximum scrolling pixels in vertical mode	FFh
Char Scrolling Disable *(4Eh-4Fh-50h)*		
SCH[17:0]	Char scrolling disable	0
Line scrolling Disable *(51h-52h-53h-54h)*		
SL[31:0]	Line scrolling disable	0
Set Sequence Character Address *(8Ah)*		
S[1:0]	Sequence number	0
N[3:0]	Character number	0
Init Sequence *(55h)*		
SEQRS	Sequence reset	0
SEQF[1:0]	Sequence frequency	0
SEQRU[4:1]	Sequence continuous mode	0
SEONCE	Sequence once run	0

Set CGRAM Address *(88h)*		
A[3:0]	Address of bitmap picture	0
Set DDRAM Address *(84h-85h)*		
RA[3:0]	Row address	0
CA[4:0]	Column address	0
Set Messages RAM address *(86h-87h)*		
MEA[3:0]	Message Address	0
CH[4:0]	Character number	0
Set Register Address *(81h)*		
RA[5:0]	Register Address	0
Set Pixels Line Address *(89h)*		
PL[4:0]	Pixels line Address	0
Set ROM Address (*82h-83h)*		
ROA[12:0]	Rom Address	0
VLCD and Bias Control *(5Ah-5Bh*)		
EN_IVLCD	Enable internal VLCD	0
VL[6:0]	VLCD level Value	0
REDUC	Voltage reduction	0
TC[1:0]	Temperature Coefficient	0
VMU[1:0]	Number of voltage multiplier stages	0
BR[2:0]	Bias Ratio	0
VLCD and VLED Control *(5Ch)*		
CK_LED	Clock LED selection	0
VLD[4:0]	VLED voltage	0
Timing Control *(5Dh)*		
EF	external rows synchronization signal enable	0
ECK	External clock enable	0
CK_VRF	Clock frequency for voltage reference	
CF[1:0]	Charge pump frequency	0
FR[2:0]	Frame frequency	2
Interrupt Mask *(59h)*		
WDOGM	Watch dog mask	0
BPROM	Bad protocol Mask	0
BDCM	Bad command interrupt Mask	0
LCDERRORM	LCD error mask	0
ESCRYM	End Scroll Mask (Y)	0
ESCRXM	End Scroll Mask (X)	0
ESEQM	End Sequence Mask	0
EBLM	End Blink Mask	0
Interrupt Clear *(80h)*		
BPROB	Bad protocol Bit	0
WDOGB	Watch dog Bit	0
BDCB	Bad command interrupt Bit	0
LCDERRORB	LCD error Bit	0
ESCRYB	End Scroll Bit	0
ESCRXB	End Scroll Bit	0
ESEQB	End Sequence Bit	0
EBLB	End Blink Bit	0
Driver/Pads Configuration *(5Eh)*		
ADIV_SEL	Active addressing divisor selection	0
AOSC_SEL	Active addressing oscillator selection	0
ADIS_RD	Active addressing read memory disable	0
AVREF_SEL	Active addressing VREF selection	0
DIS_WDOG	Watchdog disable	0
DIS_FR_P/U	Disable FR pull-up	0
EN_FR_OUT	Enable FR output	0
IRQ_PP	Enable IRQ push/pull	0
Display Mask (5Fh)		
L_ST[2:0]	Line Number Start	0
L_END[2:0]	Line Numbet End	7h

Table 10 Bits description

6.17.6 Sleep (01h)

The Sleep command put the LCD driver in Sleep mode and the main oscillator is stopped. Any new command will wake up the driver. After a sleep command, the user has to switch the display on again.

6.17.7 Clear Display (04h)

The Clear Display command writes blank characters into all DDRAM addresses. The DDRAM address counter is set to 0.

6.17.8 Return Home (03h)

The Return Home command sets the DDRAM address counter to 0.

6.17.9 Refresh (02h)

The Refresh command refreshes display with written display data if automatic refresh is disabled.
The DDRAM is double buffered. When in automatic refresh mode, DDRAM writes are periodically transferred to the LCD driver stage. When in manual refresh mode, modifications to the DDRAM have no effect until the screen is refreshed with the *Refresh* command (The manual Refresh command must be sent when the LCD is on).

6.17.10 Display Control (41h)

ACTADR	FEXCLK	AR	RR	RC	I	BI	ON

Table 11 Display Control Data field

The Display Control command configures the display.
If ACTADR is 1, the active addressing is enabled. In this case, the VLCD must be decreased, its value should be 1.59 x Vth. This addressing technique is only available for the ''one character line mode''. For active addressing, the minimum display rows number is 9.
If FEXTCLK is 1, the external clock is used for blinking, sequences and LED functions.
When AR is 1, the display is automatically refreshed.
When RR is 1, the rows outputs are mirrored to give more flexibility for LCD interconnects.
When RC is 1, the columns are mirrored.
When I is 1, the display is in inverse mode, the white pixels become black and the black ones become white.
The bit BI selects the bitmap mode. In this case, the DDRAM is automatically filled with CGRAM addresses as described in 6.20.3. The user must fill CGRAM memory.
The ON bit switches on the display. If this bit is 0, the LCD is blank.

6.17.11 LED Control (42h)

LEDINTV	LEN	L2DC2	L2DC1	L2DC0	L1DC2	L1DC1	L1DC0

Table 12 LED Control Data field

The LED control command configures the LED driver.
IF LEDINTV is 1, the internal voltage generator is used to generate the voltage for LED.
The signals generation starts when the LEN bit is 1.
The L1DC[2:0] and L2DC[2:0] bits set the LED 1 and LED 2 PWM duty cycle as follows:

LxDC[2:0]	Duty Cycle
0	0%
1	10 %
2	20 %
3	30 %
4	40 %
5	60 %
6	80 %
7	100 %

Table 13 LED duty cycle

If LEN is 0, the PWM output is set to 0.

6.17.12 Configure Mode and Line (8Ch) Free Mode

-	-	-	FMN	-	L2	L1	L0

Table 14 Set Display Line Number data field

Set Display Line number selects the free mode and the character line number. This command is used in Free Mode to select line and mode before entering its parameters.

6.17.13 Set Display Rows Number (6Fh) Free Mode

MUX1LP	MUX1DR	RN5	RN4	RN3	RN2	RN1	RN0

Table 15 Set Display Rows Number data field

This command sets the display rows number. It can also be used for consumption reduction to use only a part of the display. The Multiplexing rate is directly set by this command. The possible multiplexing rates are static, 2, 3, 4, 8, 10, 16, 20, 24, 32. All other corresponding rows values are forbidden.
For Static addressing, the bit MUX1LP chooses the configuration. If the bit MUX1LP is 0, intermediate voltages are generated for the unused rows. If this bit is 1, the 32 rows have the same signals (rows can be connected together to increase the drive capability). The MUX1DR bit disables the memory read when the text does not change.

6.17.14 Set Line Start Column (70h) Free Mode

-	X6	X5	X4	X3	X2	X1	X0

Table 16 Set Line Start Column data field

Set Line Start Column defines the Line Start Column on the display. If the parameter is 0, the first left column is selected.

6.17.15 Set Line Start Row (71h) Free Mode

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Table 17 Set Line Start Row data field

Set Line Start Row defines the Line Start Row on the display. If the parameter is 0, the first row is selected.

6.17.16 Select Character Set (72h-73h) Free Mode

CHN4	CHN3	CHN2	CHN1	CHN0	CS2	CS1	CS0
CAR2	CAR1	CAR0	CBR2	CBR1	CBR0	CH1	CH0

Table 18 Select Character Set (1) and (2) data fields

Select Character Set defines the characters number of full width per line, used character format, used cursor, cursor size and space between cursor and character. To define a number of characters, the user should write the number of character -1 in the field CHN. (The maximum is 17 characters. if CHN[4:0] is bigger or equal than 16, 17 characters will be used)The CHN parameter defines also the scrolling window (the scrolling window is equal to (CHN+1)*BW). If the cursor height (CH) is 0, the cursor function is disabled and all the parameters (CAR, CBR) in relation with this function are ignored.
The character format is defined by the CS[2:0] bits as follow:

CS[2:0]	Character Format
0	6x8
1	5x7
2	5x10
3	10x16
4	15x24

Table 19 Characters formats

CH[1:0] defines the height of the cursor.
The space between the cursor and the character is defined by the CBR[2:0] value.
The rows number after the cursor is defined by CAR[2:0].

6.17.17 Set Bitmap Width (74h) Free Mode

ZX1	ZX0	BW5	BW4	BW3	BW2	BW1	BW0

Table 20 Set Bitmap Width data field

Set Bitmap Width defines the distance between two characters (BW[5:0]) and the space (ZX[1:0]) before the character. The maximum character bitmap width is 17. If the user enters a higher BW, the driver will add blank pixels. .The parameter BW does not include ZX. In zoom 2 and zoom 3 for active addressing, the parameter BW is multiplied by 2 or by 3.

6.17.18 Set Bitmap Height (75h) Free Mode

ZY1	ZY0	BH5	BH4	BH3	BH2	BH1	BH0

Table 21 Set Bitmap Height data field

Set Bitmap Height defines the character bitmap height (BH[5:0]) and the space before the character (ZY[1:0]). The parameter BH does not include ZY and cursor parameters. For selected character format, BH is limited:
- to 8 for characters 5x7, 6x8- to 16 for characters 5x10, 10x16
- to 24 for characters 15x24

Blank lines will be added after the character until the limit defined by the character format.
If the host uses a higher BH, the character itself will be displayed again for 5x7,6x8,5x10,10x16 format. For 15x24 character, the driver will display the content of memory after the 15x24 character bitmap (actually small characters 5x7 and 6x8).

6.17.19 Select Mode (43h)

CHB	ZO1	ZO0	FM_EN	M3	M2	M1	M0

Table 22 Select Mode data field

This command selects test mode, predefined modes or free mode.
If CHB is 1, a checker board is displayed for test purpose. In this case, the DDRAM is kept (No blink function should be selected)
The bits ZO[1:0] define zoom for active addressing.
If FM_EN is 1, a free mode is activated (Two free modes are available). This means that the user must have defined all line characteristics (column and row start, characters set, columns number, rows number, bitmap width and height) before setting FM_EN to 1.The bits M[3:0] define the modes (predefined or free).

6.17.20 Blank Line (56h)

BLA8	BLA7	BLA6	BLA5	BLA4	BLA3	BLA2	BLA1

Table 23 Blank Line data field

This command blanks the lines specified by the bits BLA[8:1]. This command keeps the old DDRAM blank configuration. This command has no influence on the underline cursor and sequence.

6.17.21 Blink Line (57h)

BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1

Table 24 Blink line data field

This command blinks the lines specified by the bits BL[8:1]. The blink is displayed by switching display characters line and all line dots off with a period defined by the blink parameters (see Blink Control Command). This command keeps the old DDRAM blink configuration. This command has no influence on the underline cursor and sequence.

6.17.22 Invert Line (58h)

IL8	IL 7	IL 6	IL 5	IL 4	IL 3	IL 2	IL 1

Table 25 Invert line data field

This command inverts the lines specified by the bits IL[8:1]. This command keeps the old DDRAM invert configuration. This command has no influence on the sequence.

6.17.23 Blank Complete Line (91h)

BLACL8	BLACL 7	BLACL 6	BLACL 5	BLACL 4	BLACL 3	BLACL 2	BLACL 1

Table 26 Blank complete Line data field

This command blanks the lines specified by the bits BLACL[8:1]. The old DDRAM blank configuration is lost. This command has no influence on the underline cursor and sequence.

6.17.24 Blink Complete Line (92h)

BCL8	BCL7	BCL6	BCL5	BCL4	BCL3	BCL2	BCL1

Table 27 Blink complete Line data field

This command blinks the lines specified by the bits BCL[8:1]. The blink is displayed by switching display characters line and all line dots off with a period defined by the blink parameters (see Blink Control Command). The old DDRAM blink configuration is lost. This command has no influence on the underline cursor and sequence.

6.17.25 Invert Complete Line (94h)

ICL8	ICL 7	ICL 6	ICL5	ICL 4	ICL3	ICL2	ICL1

Table 28 Invert complete line data field

This command inverts the lines specified by the bits ICL[8:1]. The old DDRAM invert configuration is lost. This command has no influence on the sequence.

6.17.26 Picture/Character Control (99h - 98h - 9Ah)

SEQ	M	SP	C	INB	I	B	BLA

Table 29 Picture/Character Control data field

These 3 commands define actions on current character or picture.
Command *Clear Char. Control (98h)* allows clearing to 0, one or more bits.
Command *Set Char. Control (99h)* allows setting to 1, one or more of these 8 bits.
Command *Modify Char. Control (9Ah)* allows modifying in one time bits BLA, B, I, INB, C, M, SEQ and SEQ. If SEQ is 1, a sequence of character is displayed at the current location. The attributes of the Sequence character in the Sequence RAM are prioritary.
If M is 1, a message starts at the current location.
If BLA is 1, the character is blank (the ASCII code is kept in memory). This bit has no influence on the underline cursor.
When the bit I is 1, the current character is in inverse mode. The white pixels become black and the black pixels become white.
If the B bit is set, the current character blinks.
If the INB bit is set, the character blinks with its inverse.
The cursor is displayed when the C bit is 1. If B and C are set, cursor and character can blink simultaneous or in alternation (see *Cursor Control* command). The Move cursor command has no influence on the cursor or blink set by the command Set Char. Control.
If SP is 1, the current character is superposed with the character defined by the command *Write Superposition character*.
This command set the pointer to the next character. When the pointer has reached the last character, it goes after to the first character without changing line.

6.17.27 Write Superposition Character (8Eh)

SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Table 30 Write Superposition data field

This command defines the character to be superposed at the current address.

6.17.28 Read Superposition Character (AEh)

SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Table 31 Read Superposition data field

This command reads the superposed character at the current address.

6.17.29 Cursor Control (44h)

-	CFA	BFA	D/I	AU_RD	AU_WR	CIB	CB

Table 32 Cursor Control data field

The Cursor Control command defines cursor blinking mode and RAM (DDRAM, CGRAM, Messages RAM or Sequence RAM), register address move.
When the bit D/I is set, the RAM or register address is decremented. When the bit D/I is cleared, the RAM or register address is incremented.
When CFA is 1, the displayed cursor follows the DDRAM address.
When BFA is 1, the blink follows the DDRAM address.

When AU_RD is 1, RAM or register address is automatically incremented for read action (D/I = 0) or is automatically decremented (D/I=1).
When AU_WR is 1, RAM or register address is automatically incremented for write action (D/I = 0) or is automatically decremented (D/I=1).
If the bit CIB is 1, the cursor blinks in alternation with the character (if the character or line blink is enabled).
If the bit CB is 1, the cursor blinks simultaneous with the character (if the character or line blink is enabled).
If the character blink is disabled and the bit CB or CIB is set, only the cursor blinks.
For DDRAM, Messages RAM, Sequence RAM, when the address has reached the last character, it goes after to the first character without changing line, message or sequence.
For CGRAM, when the address has reached the last line, it goes after to the first line without changing CGRAM character in partial bitmap mode.

6.17.30 Move Cursor (8Dh)

-	FL	NL	PL	-	CR	MF	MB

Table 33 Move Cursor field

If the bit FL is set, the DDRAM address (or cursor, blink when CFA or BFA are set) goes to the first line.
If the bit NL is set, the DDRAM address (or cursor, blink when CFA or BFA are set) goes to the next line.
If PL is set, the DDRAM address (or cursor, blink when CFA or BFA are set) goes to the previous line.
If CR is set, the DDRAM address (or cursor, blink when CFA or BFA are set) goes to the beginning of the line.
If MF is set, the DDRAM address (or cursor, blink when CFA or BFA are set) moves forward.
If MB is set, the DDRAM address (or cursor, blink when CFA or BFA are set) moves backward.

6.17.31 Blink Control (46h)

BN2	BN1	BN0	BDC1	BDC0	BF1	BF0	BST

Table 34 Blink Control data field

The Blink Control command defines blink number, blink duty cycle and blink frequency.
If the blink number defined by the BN[2:0] bits is 0, the blink action will go on until the user clears the B bit with a Picture/Character Control command or with a Blink Line command. Otherwise, the character or line will blink the defined number by the bits BN[2:0]. The blink starts when BST is 1.
The blink duty cycle is defined with the BDC[1:0] bits as follows:

BDC[1:0]	Duty cycle
0	50%
1	25%
2	75%

Table 35 Blink duty cycle (Duty cycle ON, 100% - Duty cycle OFF)

The blink different frequencies are shown in the following table
(Values are given for a frame rate Fframe of 75Hz or for an external functional clock 32,768 kHz):

BF[1:0]	Frequency [Hz]
0	4Hz
1	2Hz
2	1Hz
3	0.5 Hz

Table 36 Blink Frequencies

For a frame rate less than 75Hz, the blink frequency is reduced by the factor Fframe/75.
These values are only accurate when the external functional clock is 32,768khz and is selected.

6.17.32 Scrolling Control (9Ch)

-	.-	SCRST	SCYST	SCXSTP	SCYSTP	SCXRS	SCYRS

Table 37 Scrolling Control data field

If the bit SCXRS is 1, the horizontal scrolling pointer is set to 0.
If the bit SCYRS is 1, the vertical scrolling pointer is set to 0.
The SCYST bit starts the scrolling once in vertical mode.
The SCXST bit starts the scrolling once in horizontal mode.
The SCYSTP bit stops the scrolling once in vertical mode.
The SCXSTP bit stops the scrolling once in horizontal mode.
The user has to wait 3*(1/Scrolling frequency) to see the result of this command or before sending this command again.

6.17.33 Scrolling Config (47h)

The Scrolling Control configures the scrolling mode.

SWCTRL	SF2	SF1	SF0	R/L	D/U	CONTX	CONTY

Table 38 Scrolling Config data field

The bits SF[2:0] set the scrolling frequency as follows:

SF[1:0]	Frequency [Hz]
0	Fframe/2
1	Fframe/4
2	Fframe/8
3	Fframe/16
4	Fframe/32
5	Fframe/64
6	Fframe/128
7	Fframe/256

Table 39 Scrolling Frequencies

The SWCTRL bit selects the function of Scrolling Max Control commands.
The R/L bit configures horizontal scrolling to right if this bit is 1.
The D/U bit configures vertical scrolling to down if this bit is 1.
If the bit CONTY is 1, the scrolling starts in continuous vertical mode.
If the bit CONTX is 1, the scrolling starts in continuous horizontal mode.
Frequency change during scrolling is not allowed (The delay of frequency switching is variable).

6.17.34 Scrolling Number Control (48h - 49h - 4Ah)

SHN7	SHN6	SHN5	SHN4	SHN3	SHN2	SHN1	SHN0
SVN7	SVN6	SVN5	SVN4	SVN3	SVN2	SVN1	SVN0
SVN11	SVN10	SVN9	SVN8	SHN11	SHN10	SHN9	SHN8

Table 40 Scrolling Number Control data field

The bits SHN[11:0] configure the number of pixels to scroll in horizontal mode.
The bits SVN[11:0] configure the number of pixels to scroll in vertical mode.

If scrolling is performed in continuous mode, this field is not used, and the display is scrolled until the Scrolling Max Control value is reached, repeating indefinitely.
If scrolling is performed in once mode, the behavior is similar as above, but when the display has been shifted by the number of pixels given by the Scrolling Number Control command (perhaps after several cycles, as defined by Scrolling Max Control), scrolling stops and an interrupt is generated.

6.17.35 Scrolling Max Control (4Bh - 4Ch - 4Dh)

MXH7	MXH 6	MXH 5	MXH 4	MXH 3	MXH 2	MXH 1	MXH 0
-	-	-	-	-	-	MXH9	MXH8
MXV7	MXV 6	MXV 5	MXV 4	MXV 3	MXV 2	MXV 1	MXV 0

Table 41 Scrolling Max Control data field

When SWCTRL bit of the Scrolling Config command is 0, the bits MXH[9:0] defines the content length to scroll in pixels in horizontal mode and the bits MXV[7:0] defines the window to scroll in pixels in vertical mode (the window starts always at coordinate 0). When the scroll pointer has reached the MXH or MXV value, the pointer goes to 0.
When SWXTRL bit is 1, the bits MXH[9:0] and the bits MXV[7:0] configures the absolute position of the scroll window.

6.17.36 Char scrolling disable (4Eh - 4Fh - 50h)

SCH17	SCH16	SCH15	SCH14	SCH13	SCH12	SCH11	SCH10
SCH9	SCH8	SCH7	SCH6	SCH5	SCH4	SCH3	SCH2
SCH1	SCH0	-	-	-	-	-	-

Table 42 Char scrolling disable data field

If the bit SCHx is 1, the scrolling in vertical mode is disabled for the character x.

6.17.37 Line scrolling disable (51h - 52h - 53h - 54h)

SL31	SL30	SL29	SL28	SL27	SL26	SL25	SL24
SL23	SL22	SL21	SL20	SL19	SL18	SL17	SL16
SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8
SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

Table 43 Line scrolling disable data field

If the bit SLx is 1, the scrolling in horizontal mode is disabled for the pixels line x.

6.17.38 Set Sequence character address (8Ah)

-	-	S1	S0	N3	N2	N1	N0

Table 44 Enter Sequence Character data field

This command set the sequence character address. 4 sequences of 16 characters can be defined. S[1:0] gives the sequence number and N[3:0] the character number.

6.17.39 Use Sequence (9Eh)

0	0	M3	M2	M1	M0	S1	S0

Table 45 Use Sequence data field

Where M[3:0] = L - 1, and L is the length of the sequence, in frames
and S[1:0] is the sequence number

6.17.40 Init Sequence (55h)

SEQRS	SEQF1	SEQF0	SEQRU4	SEQRU3	SEQRU2	SEQRU1	SEQONCE

Table 46 Init Sequence data field

This command clears the sequence buffer, initializes sequence parameters, and then starts the sequence(s).
The user has to wait one frame after the bit SEQRS has been set before sending the same command and three frames to see the action on the LCD.

For each sequence, the behavior depends on the corresponding SEQRU[i] bit, and the SEQONCE bit, according to the following truth table:

SEQRU[i]	SEQONCE	Behaviour
0	0	Do not run sequence
0	1	Run sequence once
1	0	Run sequence continuously
1	1	Run sequence continuously

Table 47 Sequence behaviour

SEQRU[4:1] runs the corresponding sequence(s) in continuous mode.
SEQONCE runs the remaining non-running sequence once.
SEQRS resets the sequence to the first character.

The bits SEQF[1:0] defines sequence frequency as follows:
(values are given for a frame rate Fframe of 75Hz or for an external functional clock 32,768kHz) :

SEQF[1:0]	Frequency
0	4Hz
1	2Hz
2	1Hz
3	0.5 Hz

Table 48 Sequence generation frequencies

These values are only accurate when the external functional clock is 32,768khz and is selected.

6.17.41 Set CGRAM Address (88h)

-	-	-	-	A3	A2	A1	A0

Table 49 Set CGRAM Address data field

Set CGRAM Address loads CGRAM addresses defined by the bits A[3:0] in the address counter. Data can be written or read from the CGRAM.

6.17.42 Set DDRAM Address (84h - 85h)

-	-	-	-	RA3	RA2	RA1	RA0
-	-	-	CA4	CA3	CA2	CA1	CA0

Table 50 Set DDRAM Address data field

Set DDRAM Address loads DDRAM addresses defined by the bits RA[3:0] and CA[4:0] in the address counter. Data can be written or read from the DDRAM.

6.17.43 Set Messages RAM Address (86h - 87h)

-	-	-	-	MEA3	MEA2	MEA1	MEA0
			CH4	CH3	CH2	CH1	CH0

Table 51 Set Messages RAM Address data field

Set Messages RAM Address loads Messages RAM addresses defined by the bits MEA[3:0] and the bits CH[4:0]in the address counter. Data can be written or read from the Messages RAM memory.

6.17.44 Use Message (9Dh)

SPM	ME6	ME5	ME4	ME3	ME2	ME1	ME0

Table 52 Use Message data field

This command set the message to use in the current selected line.
The message number is defined with the ME[6:0] bits. The first 64 messages are in ROM, the following messages are in RAM.
If SPM is 1, the message is superposed with the following message. Superposed message has length of the shorter message. If the used message is the last one and the bit SPM is 1, the message will be superposed with the first one.
This function superpose can be used to place accents on the characters of a message, for example.

The Use Message command set the Pointer to the next line if D/I is 0 otherwise to the previous line.
The Use Message command writes data only on the current DDRAM address. It allows keeping a maximum of previous data in DDRAM. The disadvantage is that horizontal scrolling is not possible with messages (the message will disappear when the first message character is not on the display). To scroll in horizontal mode, the user has to read the message and write it in DDRAM (see 6.20.8). The attribute (blink, blank, inverse, cursor, inverse blink) of the first message character affects the whole message. Attributes sequence or superpose has no effect on message. One character should be inserted between two messages (Overlapping of messages is not possible).

6.17.45 Set Register Address (81h)

-	-	-	RA4	RA3	RA2	RA1	RA0

Table 53 Set Register Address data field

Set Register Address loads Register addresses defined by the bits RA[4:0] in the address counter.

6.17.46 Set Pixels Line Address (89h)

-	-	-	PL4	PL3	PL2	PL1	PL0

Table 54 Set Pixels Line Address data field

This command set the pixels line address in the full bitmap mode (bitmap is set to 1 with Display Control command) or the CGRAM character line in partial bitmap (bitmap is set to 0 with Display Control command). In full-bitmap mode, the user must provide the pixel line number as argument to this command, followed by the *write expanded data* command and 14 data bytes to fill the complete line. In partial-bitmap mode, the user must provide the character line number as argument to this command, followed by the *write data* command, to fill character bitmap data starting at a given character line.

6.17.47 Set ROM Address (82h - 83h)

-	-	-	ROA12	ROA11	ROA10	ROA9	ROA8
ROA7	ROA6	ROA5	ROA4	ROA3	ROA2	ROA1	ROA0

Table 55 Set ROM Address

This command set the ROM address.

6.17.48 Write Data (8Fh)

This command writes summarized data (ASCII Code) in the DDRAM, Messages RAM, Sequence RAM and data in CGRAM, registers. The most recent Set Address command determines whether the CGRAM, DDRAM, register or Messages RAM is to be written.

6.17.49 Read Data (AFh)

This command reads summarized data (ASCII Code) in the DDRAM, Messages RAM, Sequence RAM and data in CGRAM, registers. The most recent Set Address command determines whether the CGRAM, DDRAM, register, Messages RAM or ROM is to be read.

6.17.50 Write expanded Data (CFh)

This command writes entire data (functions bits followed by ASCII Code, see command 9Ch, *picture/character control*, for the meaning of these special-function bits) in the DDRAM, Messages RAM , Sequence RAM and data in CGRAM, registers. The most recent Set Address command determines whether the CGRAM, DDRAM, register or Messages RAM is to be written.

6.17.51 Read expanded Data (EFh)

This command reads entire data (ASCII Code and functions bits) in the DDRAM, Messages RAM, Sequence RAM and data in CGRAM, registers. The most recent Set Address command determines whether the CGRAM, DDRAM, register, Messages RAM or ROM is to be read.

6.17.52 VLCD and BIAS Control (5Ah - 5Bh)

EN_IVLCD	VL6	VL5	VL4	VL3	VL2	VL1	VL0
TC1	TC0	REDUC	VMU1	VMU0	BR2	BR1	BR0

Table 56 VLCD and Bias Control data field

The VLCD Control selects external or internal VLCD and programs VLCD offset values.
If EN_IVLCD is 1, internal VLCD is used.
If EN_IVLCD is 0, external VLCD is used and VLCD_IN should be disconnected from VLCD_OUT.
The VL[6:0] bits set the internally generated voltage level and depends on AVREF_SEL bit (see *5Eh*)
VLCD is given by the following formula if AVREF_SEL is 0:

VLCD = 1.25 + 0.05 x VL.
Otherwise, it is given by:
VLCD = 0.625 + 0.025 x VL.
In case of external VLCD, the VL should be as follows:
If VLCD <4,4 V, VL[6:0]="0000000".
If VLCD >4,4V, VL[6:0]="1111111".
The VLCD and Bias control command selects the temperature coefficients, the VLCD multiplier stages and the bias ratio.
Due to the temperature dependency of liquid crystals viscosity, the LCD controlling voltage VLCD must be increased for lower temperatures to obtain optimal contrast. One of these coefficients is chosen depending on the crystal needs and is proportional to VLCD.
4 different temperature coefficients are available.

If AVREF_SEL is 0, the temperature coefficients are the following:

TC[1:0]	Compensation[mV/°C]
00	0
01	-0.5 x VLCD
10	-1.15 x VLCD
11	-1.80 x VLCD

Table 57 Temperature compensation

If AVREF_SEL is 1, the temperature coefficients are the following:

TC[1:0]	Compensation[mV/°C]
00	-0.5 x VLCD
01	-1.0 x VLCD
10	-2.0 x VLCD
11	-3.3 x VLCD

Table 58 Temperature compensation

VMU[1:0] sets the internal voltage multiplier factor. These bits should be chosen depending on the V_{DD} supply voltage level and the desired V_{LCD}. To have a better performance in term of consumption, the chosen number of multiplier stages should be between 1.12VLCD/VDD and 1.42VLCD/VDD

REDUC	VMU[1:0]	Voltage multiplier
1	XX	X 1
0	00	X 2
0	01	X 3
0	10	X 4
0	11	X 5

Table 59 Voltage multiplier

The BR[2:0] bits set the bias voltage ratio as follows:

BR[2:0]	Selection
000	1/3
001	1/3.5
010	1/4
011	1/4.5
100	1/5
101	1/5.5
110	1/6
111	1/6.5

Table 60 Bias ratios

The bias ratio should be done in function of the selected multiplex rate (The multiplex rate is defined with the Set Display Row Number).

6.17.53 VLED Control (5Ch)

-	CK_LD1	CK_LD0	VLD4	VLD3	VLD2	VLD1	VLD0

Table 61 VLED Control

Bit CK_LD[1:0] select the frequency f(clk_led) of the clock for the VLED DC/DC converter :

CK_LD1	CK_LD0	clk_led
0	0	Fref/8
0	1	Fref/4
1	0	Fref/2
1	1	Fref

Table 62 CK_LED frequencies

The VLD[4:0] bits set the internally generated voltage level for LED driver.
VLED is given by the following formula:
VLED = 3.7 + 0.05 x VLD.

6.17.54 Timing Control (5Dh)

EF	ECK	CK_VRF	CF1	CF0	FR2	FR1	FR0

Table 63 Timing Control data field

The Timing Control command selects external or internal clock, defines refresh and charge pump frequencies.
If the bit EF is 1, the external rows synchronization signal is used.
If the bit ECK is 1, the external clock is used. The clock should be present before setting this bit.

Bit CK_VRF select the frequency f(clk_vref) of the clock for the reference voltage device :
If CK_VRF is 0, f(clk_vref) = Fref/128
If CK_VRF is 1, f(clk_vref) = Fref/64

The CF[1:0] bits set the charge pump working frequency for the voltage doubler in low voltage configuration (clk_vcp), for the VLCD voltage multiplier (clk_mult) and for the voltage booster (clk_boost) :

CF[1]	CF[0]	clk_vcp	clk_mult	clk_boost
0	0	Fref/32	Fref/32	Fref/8
0	1	Fref/16	Fref/16	Fref/4
1	0	Fref/8	Fref/8	Fref/2
1	1	Fref/4	Fref/4	Fref

Table 64 Charge pump frequencies

The bits FR[2:0] defines refresh frequency or frame rate as follows:

FR[2:0]	Frame Rate [Hz]
000	75
001	69
010	63
011	57
100	51
101	45
110	39
111	33

Table 65 Refresh frequencies

6.17.55 Interrupt Mask (59h)

If the bit WDOGM is 1, the interrupt occurs when the watchdog enters in action (it should never occur).
If the bit BPROM is 1, the interrupt occurs when a protocol problem occurs.
If the bit LCDERRORM is 1, the interrupt occurs when an LCD error occurs.
If the bit BCM is 1, the interrupt occurs when a bad command has been sent.
If the bit ESCRXM or ESCRYM is 1, the interrupt occurs when the scrolling is finished (in once mode only).
If the bit ESEQM is 1, the interrupt occurs when the sequence is finished.
If the bit EBLM is 1, the interrupt occurs when the blink is finished (in once mode only).

WDOGM	LCDERRORM	BPROM	BCM	ESCRXM	ESCRYM	ESEQM	EBLM

Table 66 Interrupt Mask

For the sequence, the interrupt occurs at the end of the sequence after a stop in continuous mode or in once mode.

6.17.56 Interrupt Clear (80h)

This command clears the interrupt (the user must enter a 1 to clear an interrupt).

WDOGB	LCDERRORB	BPROB	BCB	ESCRXB	ESCRYB	ESEQB	EBLB

Table 67 Interrupt clear

6.17.57 Get Interrupt Status (9Fh)

This command gives the status of the LCD driver. If an error has occurred or an action is finished, the line IRQ is set to high. The user can be informed of the LCD driver status by sending the command Get Interrupt Status.

WDOG	LCDERROR	BPRO	BC	ESCRX	ESCRY	ESEQ	EBL

Table 68 Get Interrupt Status

The line IRQ is automatically set to low when all bits have been cleared with the Interrupt Clear command.

6.17.58 Auto Display (05h)

This command fills DDRAM with predefined contents to test display and its connections as follows:

		Char Nb (DDRAM Addr C[4..0])													
Line (DDRAM Addr R[2..0])	Addr	*0h*	*1h*	*2h*	..	*Dh*	*Eh*	*Fh*	*10h*	*11h*	*12h*	..	*1Dh*	*1Eh*	*1Fh*
	0h	0040h	0241h	0042h	..	024Dh	004Eh	024Fh	0040h	0241h	0042h		024Dh	004Eh	024Fh
	1h	0450h	0651h	0452h	..	065Dh	045Eh	065Fh	0450h	0651h	0452h	..	065Dh	045Eh	065Fh
	2h	0060h	0261h	0062h	..	026Dh	006Eh	026Fh	0060h	0261h	0062h	..	026Dh	006Eh	026Fh
	3h	0470h	0671h	0472h	..	067Dh	047Eh	067Fh	0470h	0671h	0472h	..	067Dh	047Eh	067Fh
	4h	0040h	0241h	0042h	..	024Dh	004Eh	024Fh	0040h	0241h	0042h		024Dh	004Eh	024Fh
	5h	0450h	0651h	0452h	..	065Dh	045Eh	065Fh	0450h	0651h	0452h	..	065Dh	045Eh	065Fh
	6h	0060h	0261h	0062h	..	026Dh	006Eh	026Fh	0060h	0261h	0062h	..	026Dh	006Eh	026Fh
	7h	0470h	0671h	0472h	..	067Dh	047Eh	067Fh	0470h	0671h	0472h	..	067Dh	047Eh	067Fh

Table 69 Auto Display DDRAM contents

6.17.59 Driver/Pads Configuration (5Eh)

This command configures watchdog, IRQ, FR pads, oscillator and voltage reference.

ADIV_SEL	AOSC_SEL	ADIS_RD	AVREF_SEL	DIS_WDOG	DIS_FR_P/U	EN_FR_OUT	IRQ_PP

Table 70 Driver/Pads Configuration

If AOSC_SEL is 0, the 256 kHz to 576 kHz frequency range is used. In active addressing with no additional functions, with a non-changing text and bit ADIS_RD set to 1 the frequency can be decreased. To use the 54 kHz minimal frequency, the bit AOSC_SEL must be 1 and the FR bits should be programmed with “110” value. If AOSC_SEL is 1 and FR is “111”, 256 kHz frequency is selected.

If ADIS_RD is 1 and in Active addressing mode, the read in memories are stopped if the content in DDRAM or the mode does not change and the blink, sequence, scrolling functions are always disabled.

AVREF_SEL selects the voltage reference. If this bit is 0, the standard Voltage reference is selected. Otherwise, a less accurate voltage reference is used. This less accurate voltage reference can be used in active addressing to reduce power consumption.

If the bit ADIV_SEL is 1, the frequency of the pads patterns (in Active addressing only) is divided by 2.

If the bit DIS_WDOG is 1, the internal watchdog is disabled. The watchdog is used only for test purpose. It is activated after 8192 clocks when a command has been sent and no answer has been received. The watchdog resets the communication interface (all data in RAM, registers are kept). This situation should never happen with a totally functional chip.

The bits DIS_FR_P/U, EN_FR_OUT configure FR pad. When DIS_FR_P/U is 0, the signal FR is internally maintained to 1. When EN_FR_OUT is 1, the FR signal is on output PFR (DIS_FR_P/U should be 1 in this case).

RQ_PP configures IRQ (Push-Pull).

6.17.60 Display mask (5Fh)

-	LST2	LST1	LST0	-	LEND2	LEND1	LEND0

Table 71 Display mask

This command set parameters line start and end for global display command (Clear Display, Auto Display, Blank complete line, Blink complete line and Invert complete line).

6.18 Operating principle

The LCD driver tasks are the ASCII codes storage, the bitmap pictures building from the ASCII codes and the multiplex or active addressing signals generation. The ASCII codes are stored in DDRAM. The bitmap pictures are built from CGROM and CGRAM and parameters.
The display signals generating are done pixel row by pixel row from the LCD driver shift register, voltages generator and parameters.

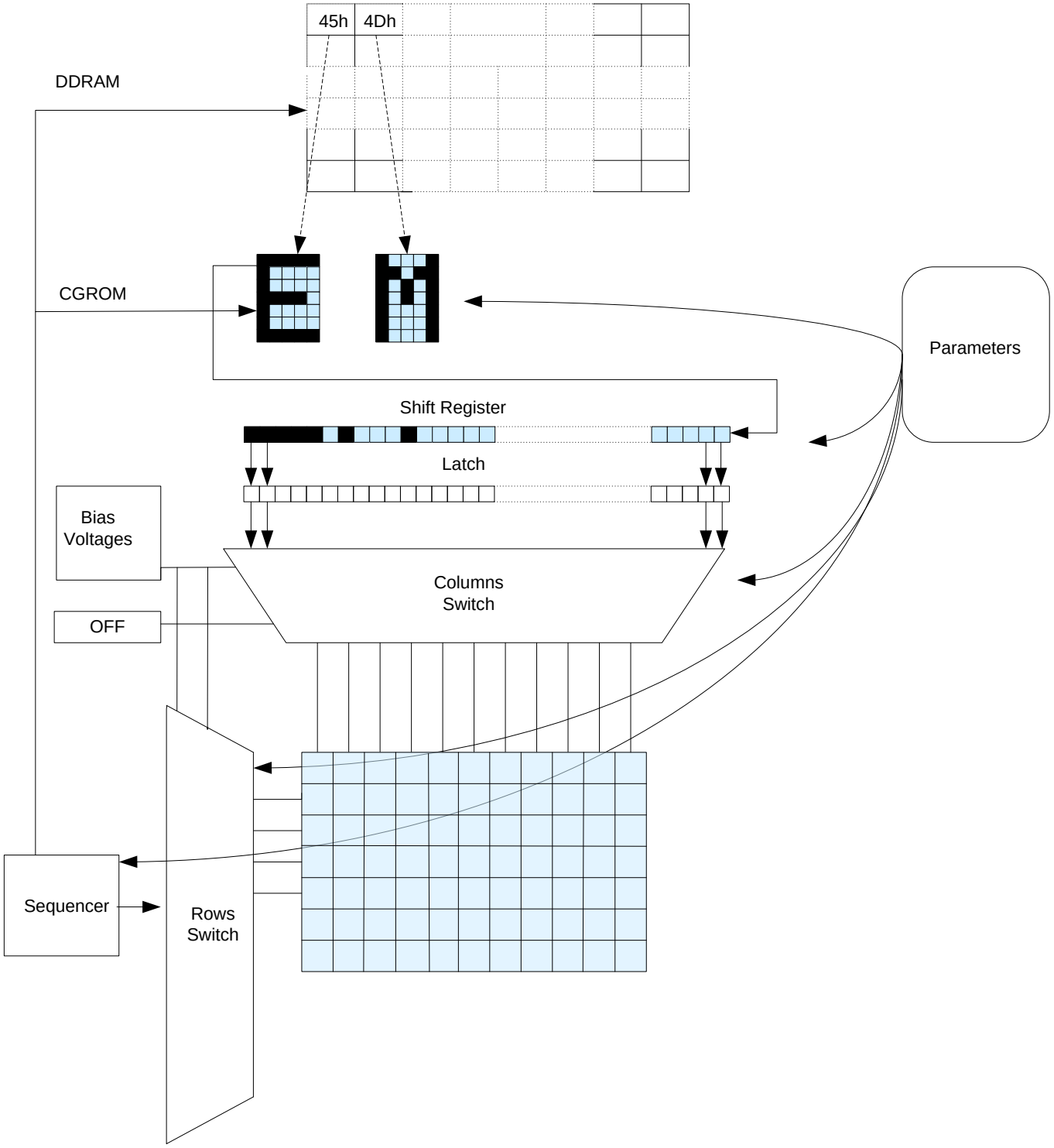


Figure 22 Operating principle

Each column or row can be turned off depending on the entered parameters (display columns number and display rows number).

6.19 Parameters

6.19.1 Modes description

16 different predefined modes and two free modes are included in the LCD driver (examples are described in appendix). Each mode contains parameters of 8 character lines maximum. For each line, pixel row and column start, bitmap width and height, character format are defined. If the line is not used, all parameters are 0.

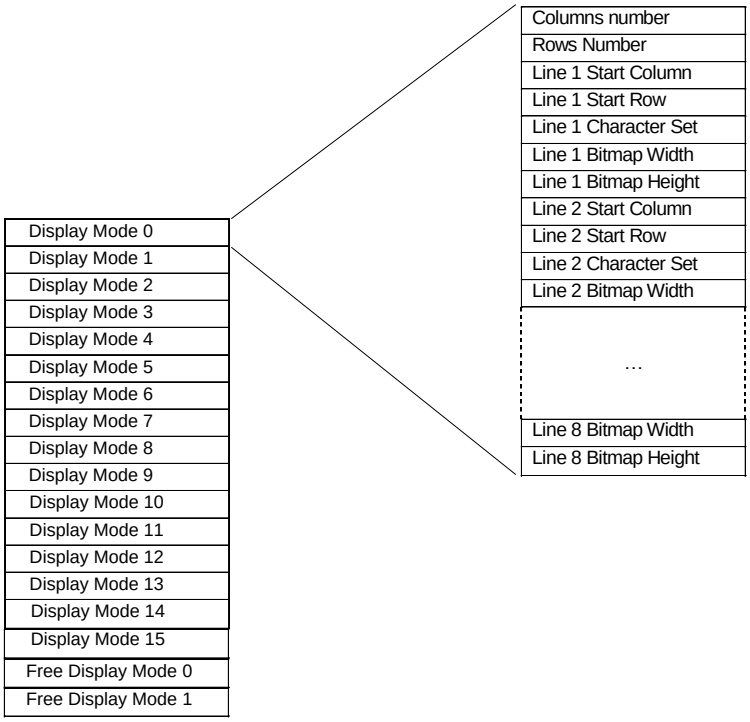


Figure 23 Mode definition

A predefined mode or a free mode is selected with the Select Mode command.

The parameters are defined as follows:

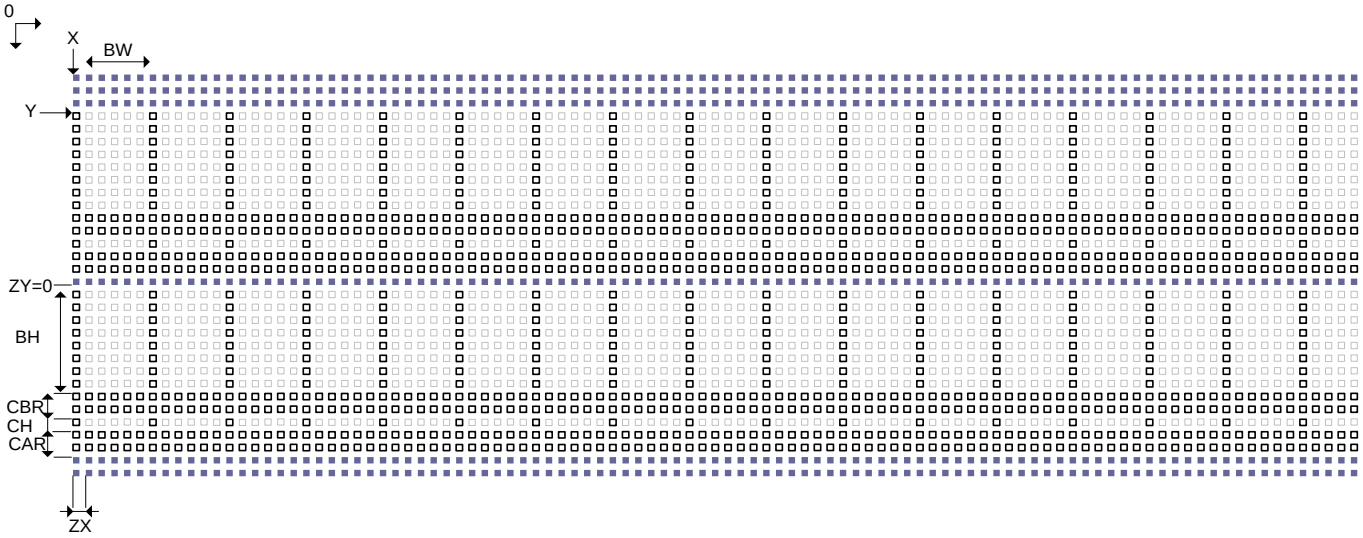


Figure 24 Mode Parameters definition

Where:

X: Start column
Y: Start row
BW: Bitmap width
BH: Bitmap height
ZX, ZY: Spaces before character
CBR: Space between character and cursor
CH: Cursor height
CAR: Space after cursor

6.19.2 Parameters list

The mode selection, VLCD (if internally generated), Bias ratio, number of voltage multipliers have to be configured by the user.

The display parameters are the following:

Display Parameters
Mode definition
VLCD selection if internal
VLCD offset value
Temperature coefficients
Bias Ratio
Number of multiplier stages for VLCD generation
Charge pump frequency
Refresh frequency

Table 72 Display parameters

6.20 Functions description

6.20.1 Reverse Columns and Rows (Command Display Control)

Rows and Columns driver pads can be mirrored to give more flexibility to LCD interconnects. In the reverse columns mode, the driver reads DDRAM and CGRAM or CGROM from right to left. In the reverse rows mode, the driver reads DDRAM and CGRAM or CGROM from bottom to top. These commands are available for the whole display.

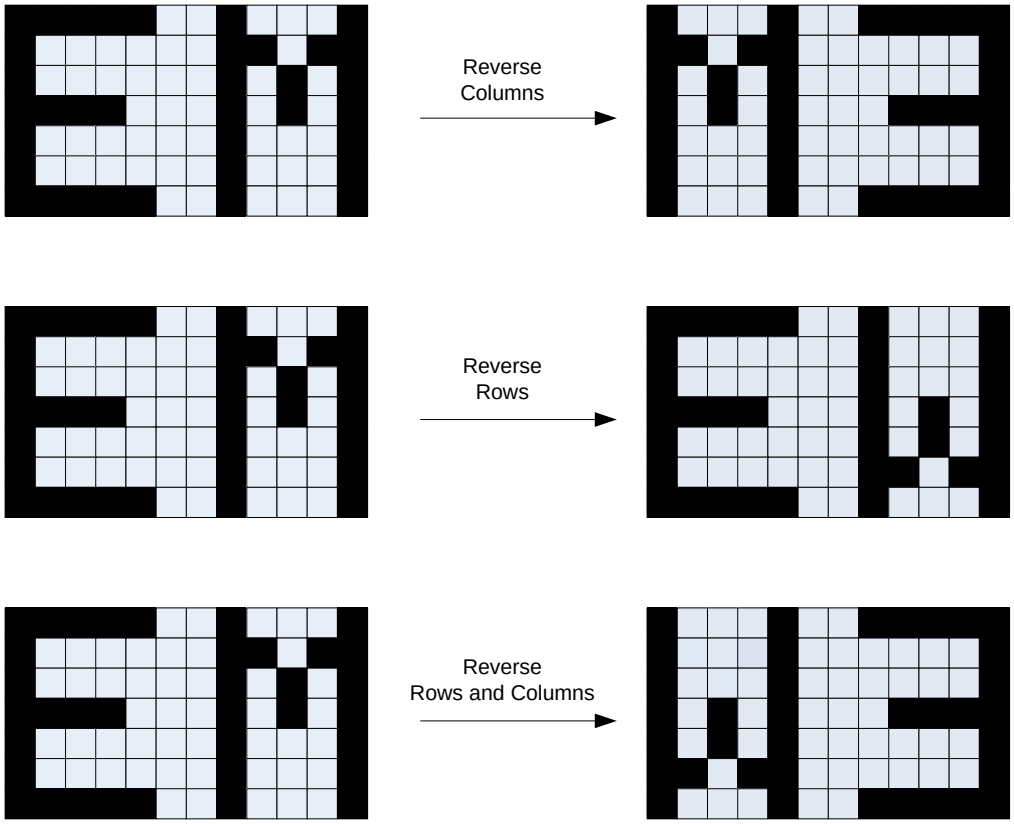


Figure 25 Reverse Rows and Columns commands

These functions are activated by setting the bits RR (Reverse Rows) and RC (Reverse Columns).

6.20.2 Inverse mode (Commands Display Control and Picture or Character Control)

In inverse mode, the OFF pixels become ON pixels and the ON pixels become OFF pixels.
The inverse mode can be used for the whole display, for a line or for a character only.

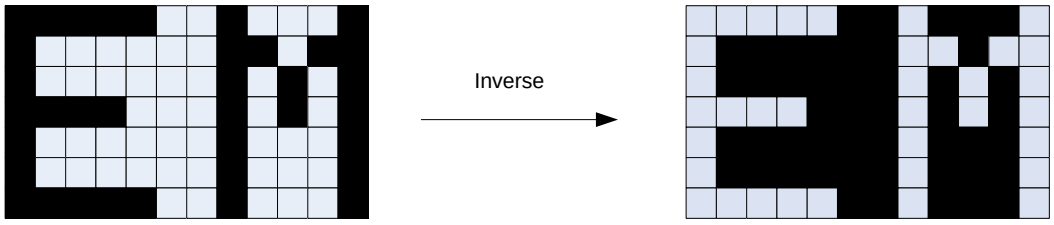


Figure 26 Inverse command

This function is activated with the command Display Control for the entire display (bit I), with the command Invert Line for a line (bits IL[8:1]) or with the Picture/Character Control command (bit I) for a character. The user must take care that the space between an inverse character and a non inverse character is sufficient to have a correct result.

6.20.3 Bitmap (Commands Display Control and Picture or Character Control)

The bitmap mode can be used for the whole display or for a character only. In bitmap mode,
the CGRAM is used.
To enter a character in bitmap mode, the user must write in the DDRAM memory a value between 00h and 0Fh, selects a CGRAM address between 00h and 0Fh, set a pixel line and write expanded data. The bitmap picture of 16x32 is filled row by row. Only a part of the picture will be displayed if the selected mode defines a smaller character size.

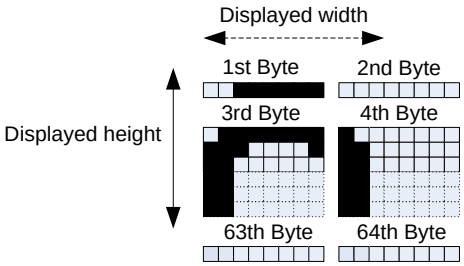


Figure 27 Bitmap picture

If the bit BI is set with the command Display Control, the DDRAM is automatically filled with CGRAM addresses as follows:

	x00000b	x00001b	x00010b	x00011b	x00100b	X00101b	X00110b	X…..b	x01111b
0000xb	00h	01h	02h	03h	04h	05h	06h	..	0Fh
0001xb	xx	xx	xx	xx	xx	xx	xx	..	xx
..	xx	xx	xx	xx	xx	xx	xx	..	xx
0111xb	xx	xx	xx	Xx	xx	xx	xx	..	xx

The user must then fill the display row by row after setting the Pixels Line Address (Command 89h).
The horizontal scroll window is limited to 256 pixels and the vertical scroll window is maximum 32 pixels.

6.20.4 Scrolling (Command Scrolling Control)

The scrolling is done pixel by pixel on the defined pixels number. The scrolling function is achieved changing the correspondence between the rows or columns of the logical memory map and the output rows or columns drivers. The scroll function doesn't affect the DDRAM content. After every scrolling, the offset between the memory address and the display pointer is incremented or decremented by one.

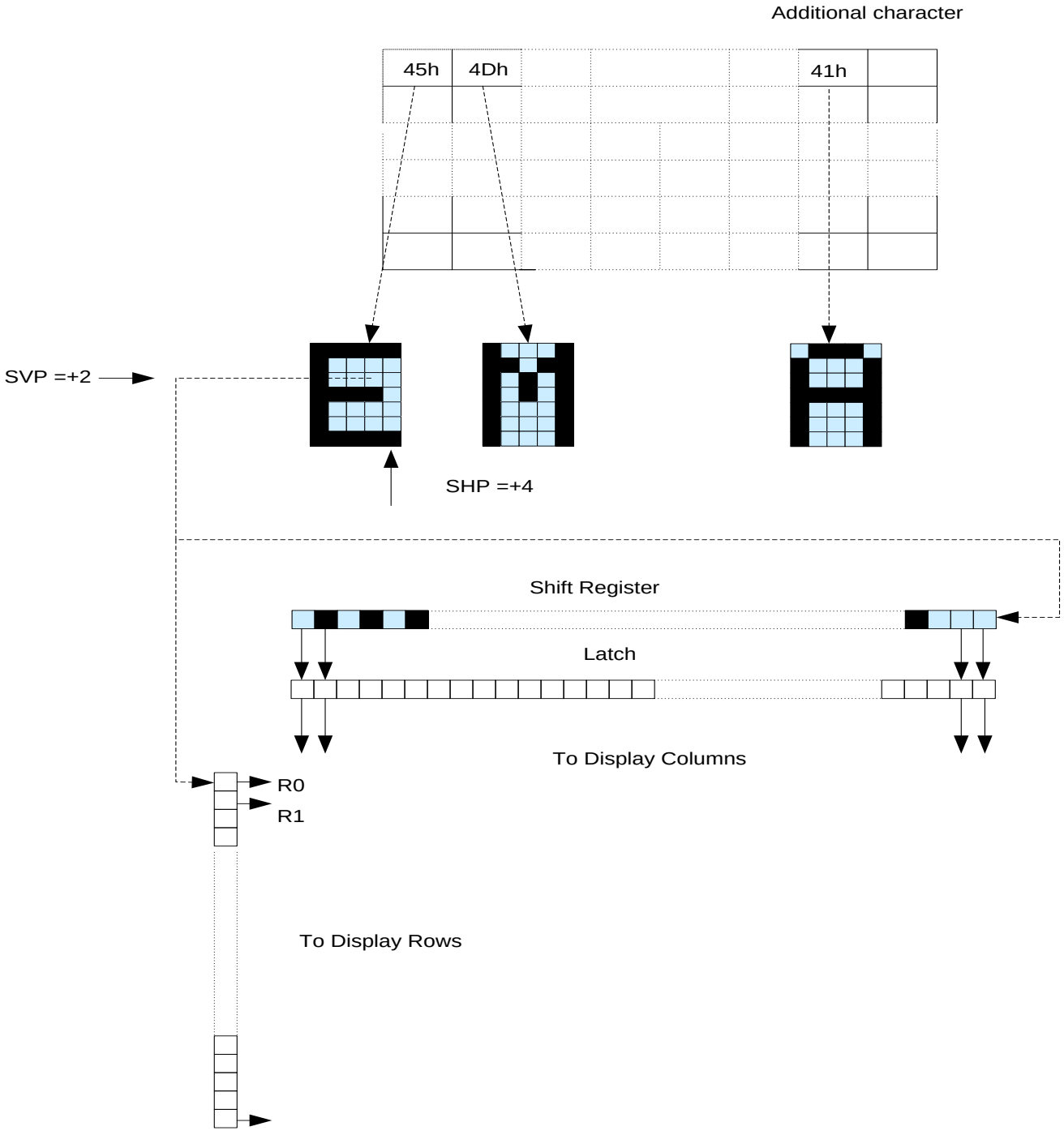


Figure 28 Scrolling function

Scrolling horizontal and vertical have different behaviors:

Scrolling horizontal and Scrolling vertical in active addressing keep the area defined in the mode

Scrolling vertical in MUX mode (several lines possible) scrolls the whole display defined in zone 0- MXV (blank lines between characters are also moving)

MXV defines the vertical scrolling range (rows 0-MXV), MXH defines maximal value of scrolling pointer (all line is moving)

Before activating the scrolling, the user must fill the non-displayed DDRAM. When the scrolling pointer has scanned the whole display, it is set to 0. When the scrolling is started in once mode, an interrupt is generated if the corresponding mask is set. Activating horizontal and vertical scrolling is possible in full scrolling mode (Line and Char Scrolling Disable set to 0) or in Partial mode. Before activating the scrolling, the user must fill the Scrolling Maximum parameters with the commands Scrolling Max Control. These parameters define when the scrolling pointer should be initialized.

The software mode (SWCTRL=1) is also possible. In this case, the Scrolling Max parameters define the absolute value of the scrolling pointer.

Some LCD displays are slow and blurring effects can appear during scrolling. To reduce these problems, the users can reduce Bias Ratio and VLCD.

6.20.5 Cursor (Command Character or Picture Control)

The cursor is applied to the current DDRAM address. It is displayed if the C bit is set with the Character or Picture command and is defined in the mode. If the bit AU_WR is 1 and D/I is 0, the cursor is displayed in the next character position. If AU_WR is 0, the cursor stays at the current location. The Cursor Control command allows moving the cursor in all directions.

6.20.6 Blink (Command Character or Picture Control)

The blink function can be done on a character or a line. Different combinations are possible when the Cursor is also activated. The character blinks and the cursor does not if B and C are set with the Character or Picture Command and CIB, CB are 0.

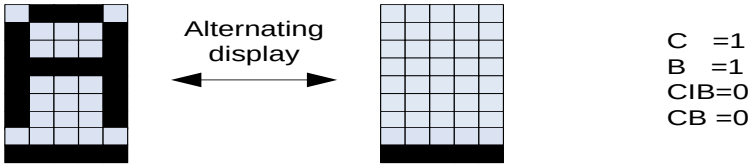


Figure 29 Cursor and blink (OR Function)

The cursor blinks and the character does not if B is 0, C is 1, CIB is 0 and CB is 1.

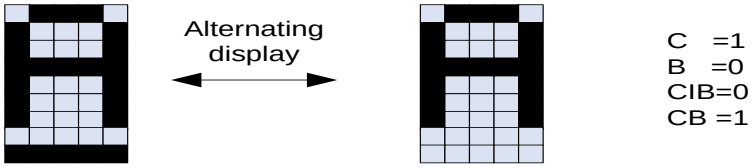


Figure 30 Cursor and blink (OR Function)

The cursor and the character blink if B is 1, C is 1, CIB is 0 and CB is 1.

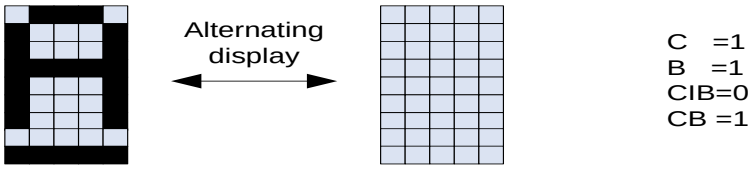


Figure 31 Cursor and blink (AND Function)

The cursor and the character blink alternately if B is 1, C is 1, CIB is 1 and CB is 0.

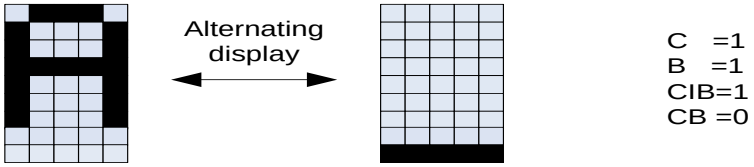


Figure 32 Cursor and blink (XOR Function)

If CIB and CB are 1, the cursor does not blink.

6.20.7 Character superposition (Command Character or Picture Control)

Character superposition is available for all characters.
To superpose a character, the user must enter the character to superpose with the Write Superposition Character and set the bit SP with the command Picture/Character Control.

6.20.8 Messages

To use a message, the user must set a DDRAM address to define the starting location of the message and select the message with the command Use Message.
The first 64 messages are in ROM, the following messages are in RAM. If SPM is 1, the message is superposed with the following message. This can be used to place accents on the characters of a message, for example.
To enter a message in the RAM, the user must set the message address and then write the data with the write data command. A message is finished with a byte 00h.
For horizontal scrolling with message, the user has to read the message and write it in DDDRAM and Superposition RAM for superposed message.
To read a message in ROM:
the user has to set the ROM address as follows: 1800h + 10h x Message Number
read message with read expanded data command until the 00h byte
To read a message in RAM:

the user has to use the command Set Message RAM address
- read message with read data command until the 00h byte

6.20.9 Sequence generation (Commands Enter Sequence Character *and* Init Sequence)

It is possible to simultaneously play up to four sequences of sixteen frames, at different character addresses in DDRAM. Four different frame rates are available, and some sequences can run in one-shot mode, while others run continuously. The SEQ special function bit indicates that a sequence is to appear instead of a character, and instead of an ASCII code, a sequence identifier byte is used. To program a sequence, the user must:
- Program the contents of the sequence(s) by executing the *Set sequence character address (8Ah)* command, followed by the sequence number, and then the *write data (8Fh)* command followed by the CGROM or CGRAM address of the characters in the sequence
- Place the following special function byte (see above paragraph), and sequence identifier byte in the DDRAM at the place where the sequence must appear:
Special function byte: 40h
Sequence identifier byte:

0	0	M3	M2	M1	M0	S1	S0

where M[3:0] = L - 1, and L is the length of the sequence, in frames
and S[1:0] is the sequence number - Start the sequence with the *Init Sequence (55h)* command.

6.20.10 Checkerboard and inverse checkerboard test functions (Command Select Mode)

This mode is activated by setting the bit CHB (Checker board) in the Select Mode register. Setting the I-bit in the Display Control register inverts the checkerboard. The checkerboard test mode does not affect the internal RAM.

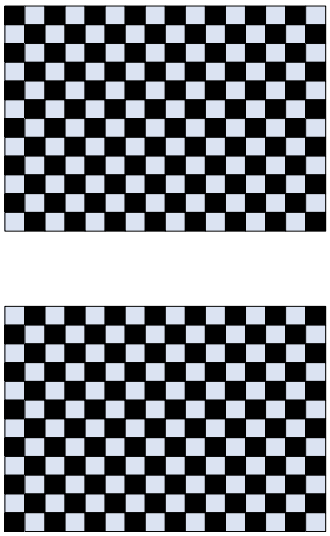


Figure 33 Checkerboard and Inverse checkerboard test pattern

7 EM6127 EXTERNAL CONNECTIONS

7.1 External capacitors for on-chip VLCD generation

The LCD driver generates on-chip VLCD voltage using 5 external capacitors. The recommended values for the external components are:

Component	Min.	Typ.	Max
CVLCD		1 µF	
C1, C2, C3, C4		100 nF	

Table 73 External capacitors values

The connection should be as follows:

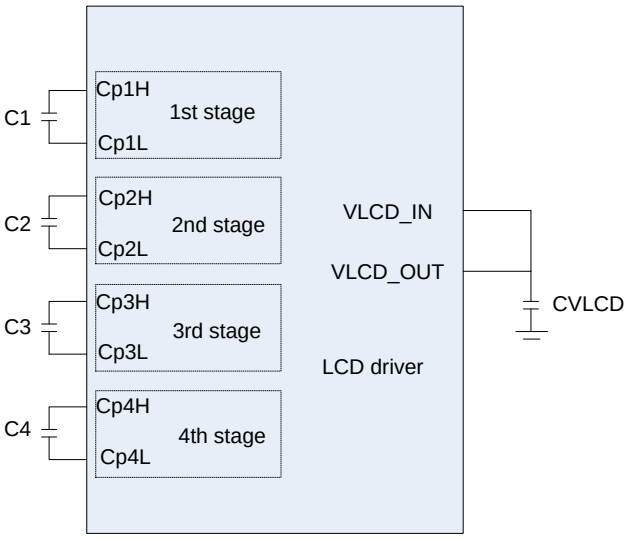


Figure 34 External capacitors connection

Series resistances between pad VLCD_IN and CVLCD and between VLCD_OUT and CVLCD should be similar.

7.2 External VLCD configuration

If an external VLCD is used, the connection should be as follows:

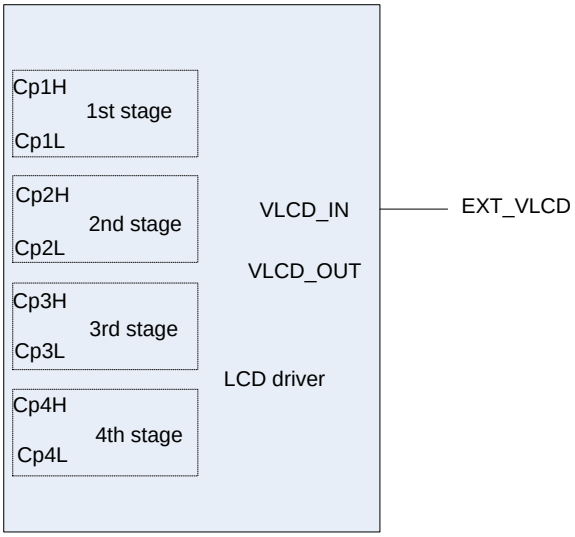


Figure 35 External VLCD connection

7.3 Configurations

Two configurations are possible:

- the low supply voltage configuration (1.2 to 2V)
- the standard configuration (2V to 3.6V)

The desired configuration is selectable via the pad LSV.
For all configurations, series resistance on VDD should not exceed 20 Ohms. The recommended values for the external components are:

Component	Min.	Typ.	Max
CDD		10 µF	
CA, CC, CD, CP		100 nF	
CB		47nF	

Table 74 External capacitors values

7.3.1 Low supply voltage configuration (1.2V to 2V)

In this case LSV is connected to VDD and an additional internal voltage booster is used. The internal regulator for digital part is not used. The connection should be as follows:

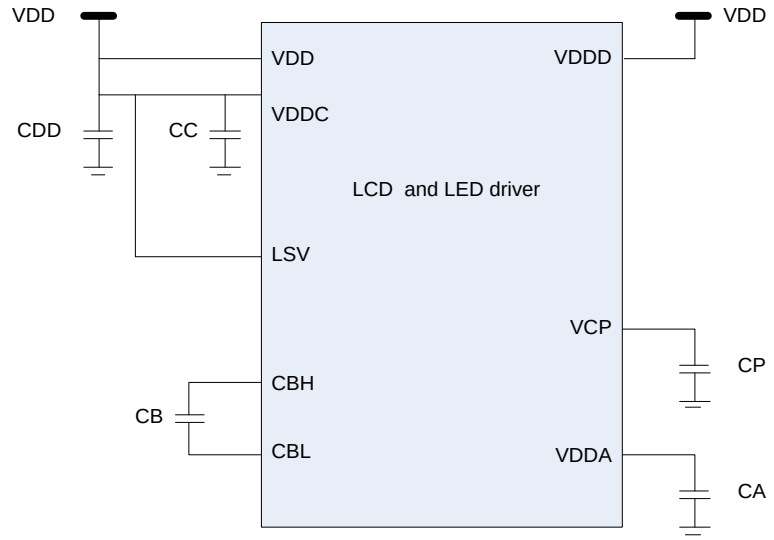


Figure 36 Low supply voltage configuration

7.3.2 Standard configuration (2V to 3.6V)

In this case, LSV is connected to ground. The voltage booster is not used and CBH, CBL are opened. The regulator for digital part is used. The connection should be as follows:

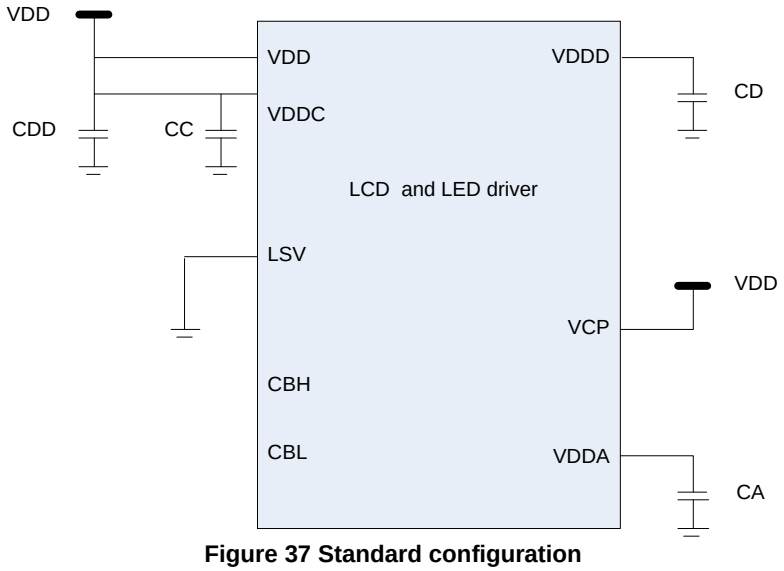


Figure 37 Standard configuration

8 ANNEXES

8.1 MODES

16 predefined modes are available. The figures defined in the following paragraphs shows different types of zone as follows:

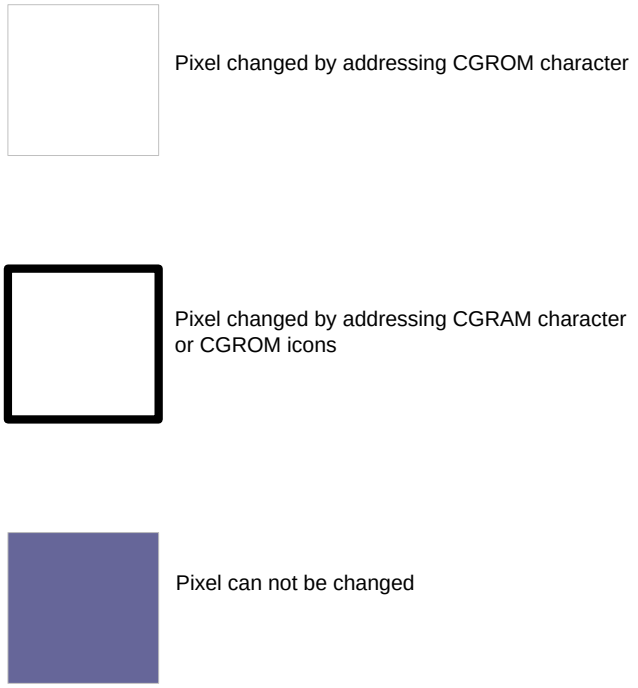


Figure 38 pixels definition

8.1.1 Mode 0: 1 line of 11 characters (5x7 visible dots) each

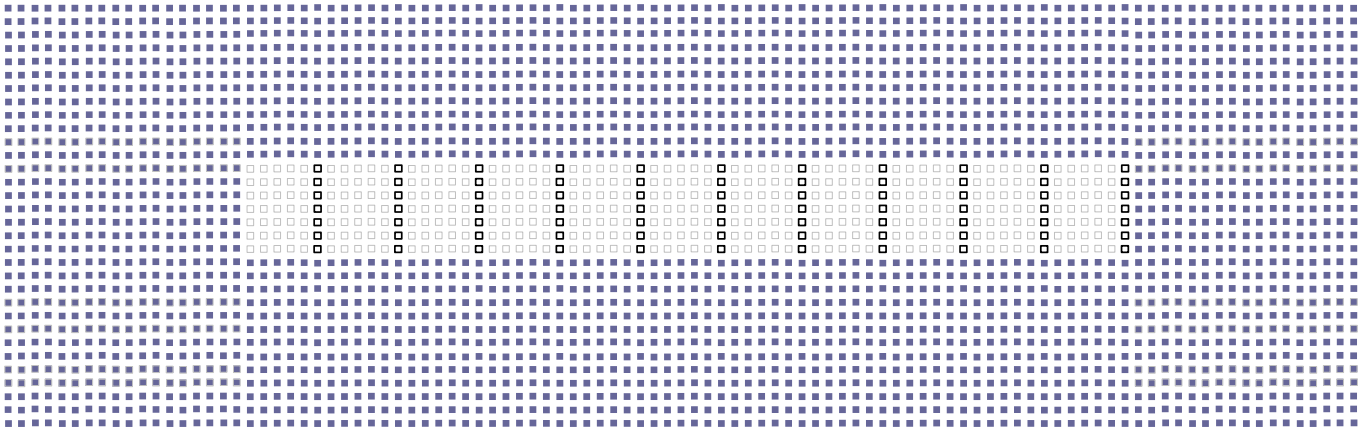


Figure 39 Mode 0 display

Columns number: 101
Rows number: 9

Line	Parameters	Value
1	Line Start Column	18
	Line Start Row	12
	Character Set	1
	Bitmap Width	6
	Bitmap Height	7

Table 75 Mode 0 parameters

8.1.2 Mode 1: 4 lines of 17 characters (5x7 dots) each

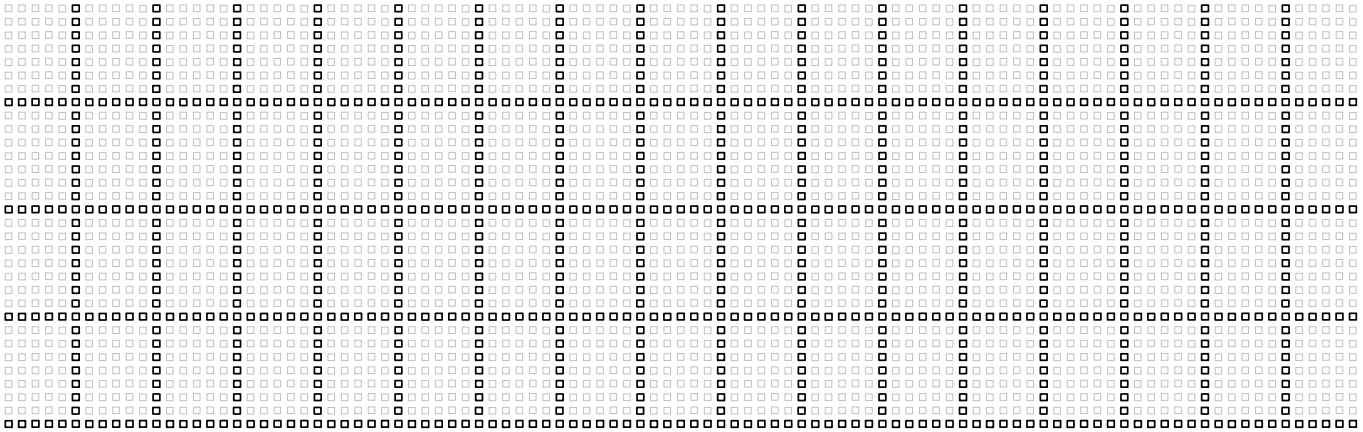


Figure 40 Mode 1 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	0
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8
2	Line Start Column	0
	Line Start Row	8
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8
3	Line Start Column	0
	Line Start Row	16
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8
4	Line Start Column	0
	Line Start Row	24
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8

Table 76 Mode 1 definition

8.1.3 Mode 2: 3 lines of 17 characters (5x7 dots) each

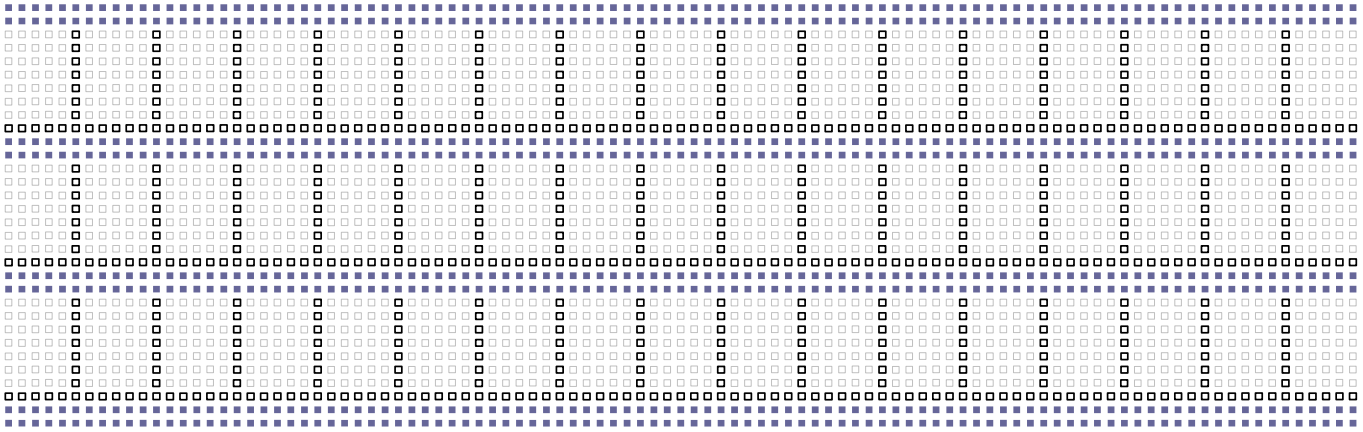


Figure 41 Mode 2 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	2
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8
2	Line Start Column	0
	Line Start Row	12
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8
3	Line Start Column	0
	Line Start Row	22
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8

Table 77 Mode 2 definition

8.1.4 Mode 3: 2 lines of 17 characters (5x10 visible dots) each

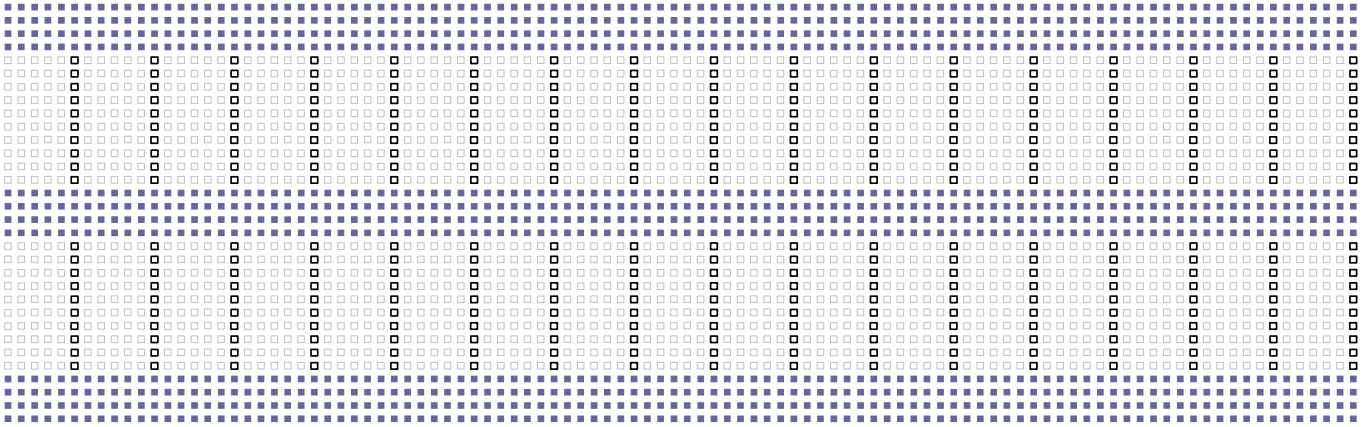


Figure 42 Mode 3 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	4
	Character Set	2
	Bitmap Width	6
	Bitmap Height	10
2	Line Start Column	0
	Line Start Row	18
	Character Set	2
	Bitmap Width	6
	Bitmap Height	10

Table 78 Mode 3 definition

8.1.5 Mode 4: 1 line of 6 characters (15x24 visible dots)

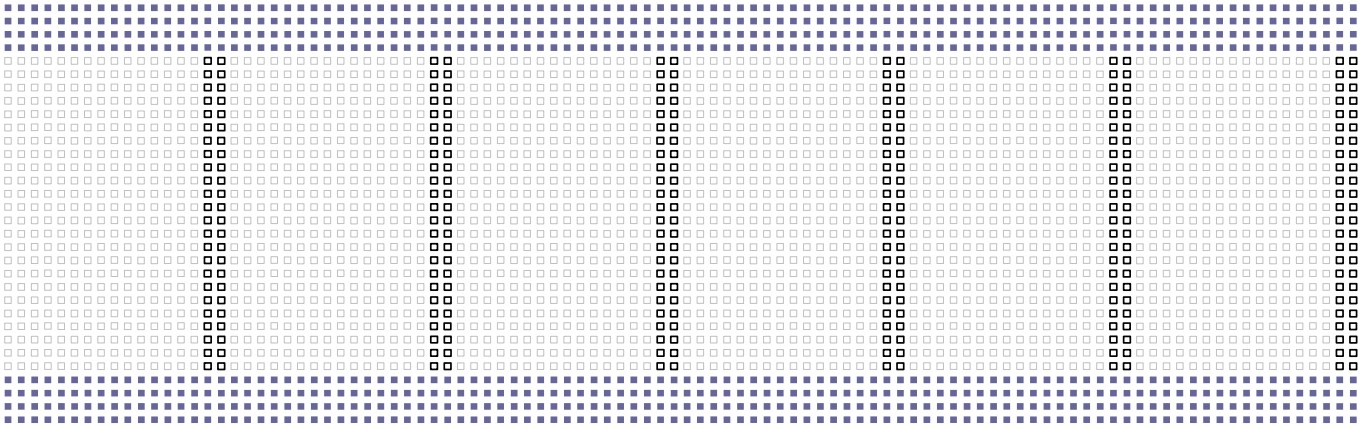


Figure 43 Mode 4 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	4
	Character Set	4
	Bitmap Width	17
	Bitmap Height	24

Table 79 Mode 4 definition

8.1.6 Mode 5: 1 line of 9 characters (10x16 visible dots) each

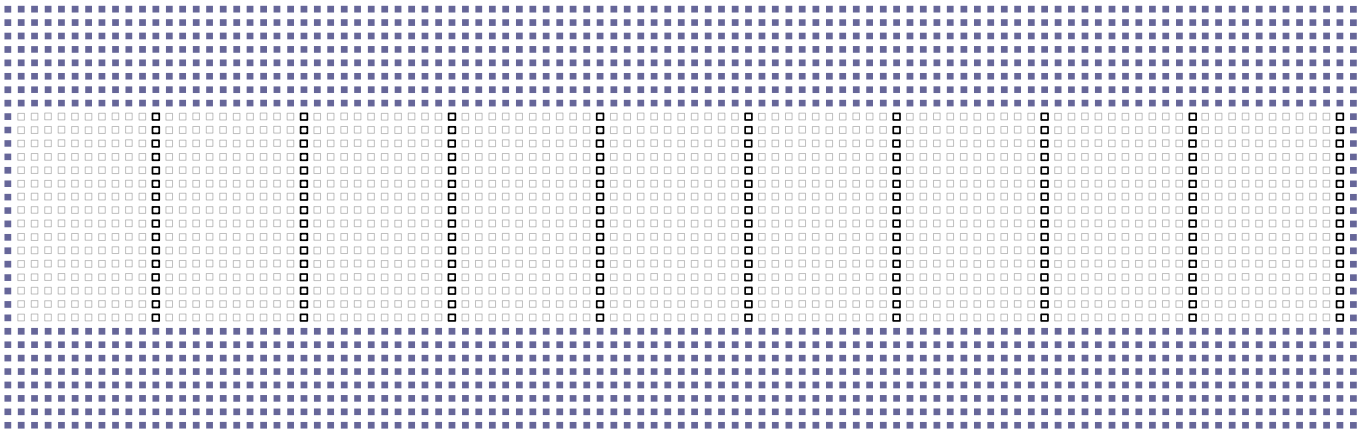


Figure 44 Mode 5 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	1
	Line Start Row	8
	Character Set	3
	Bitmap Width	11
	Bitmap Height	16

Table 80 Mode 5 definition

8.1.7 Mode 6: 3 lines of 17 characters (5x7) with cursors

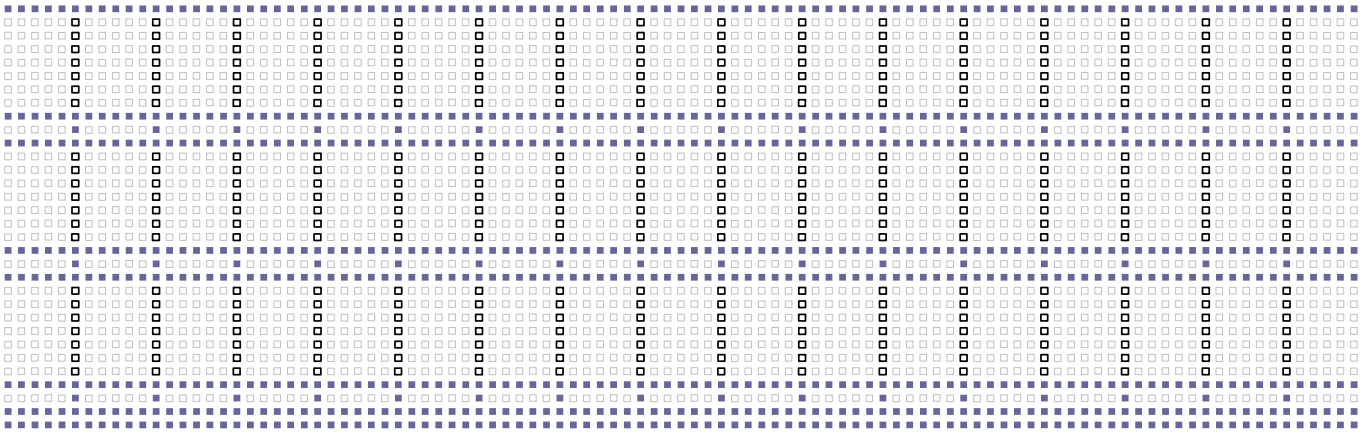


Figure 45 Mode 6 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	1
	Character Set	1
	Bitmap Width	6
	Bitmap Height	7
2	Line Start Column	0
	Line Start Row	11
	Character Set	1
	Bitmap Width	6
	Bitmap Height	7
3	Line Start Column	0
	Line Start Row	21
	Character Set	1
	Bitmap Width	6
	Bitmap Height	7

Table 81 Mode 6 parameters

8.1.8 Mode 7: 2 lines of 17 characters (5x7 dots) with cursors

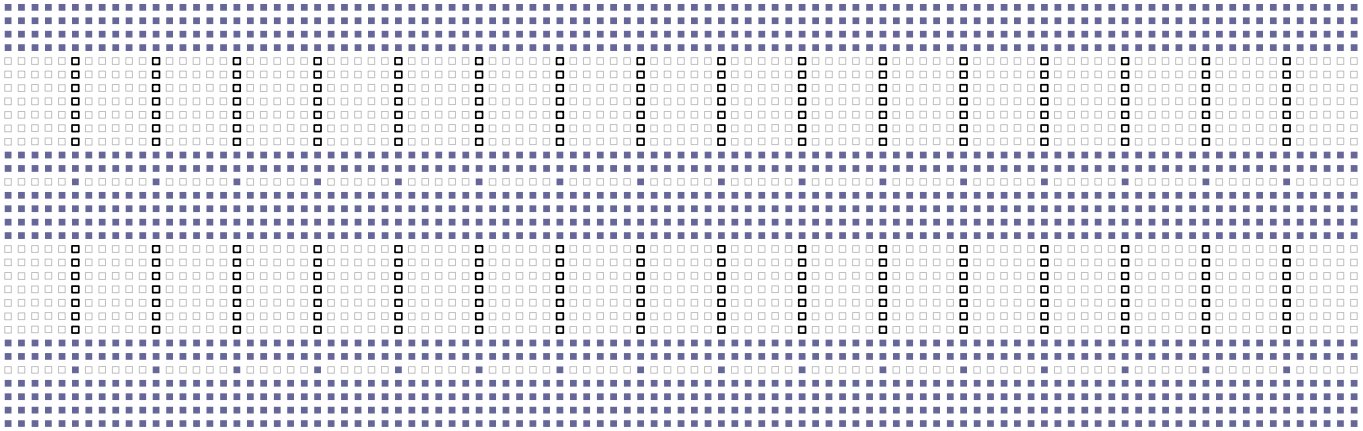


Figure 46 Mode 7 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	4
	Character Set	1
	Bitmap Width	6
	Bitmap Height	7
2	Line Start Column	0
	Line Start Row	18
	Character Set	1
	Bitmap Width	6
	Bitmap Height	7

Table 82 Mode 7 parameters

8.1.9 Mode 8: 1 line of 9 characters (10 x16 dots) with cursors

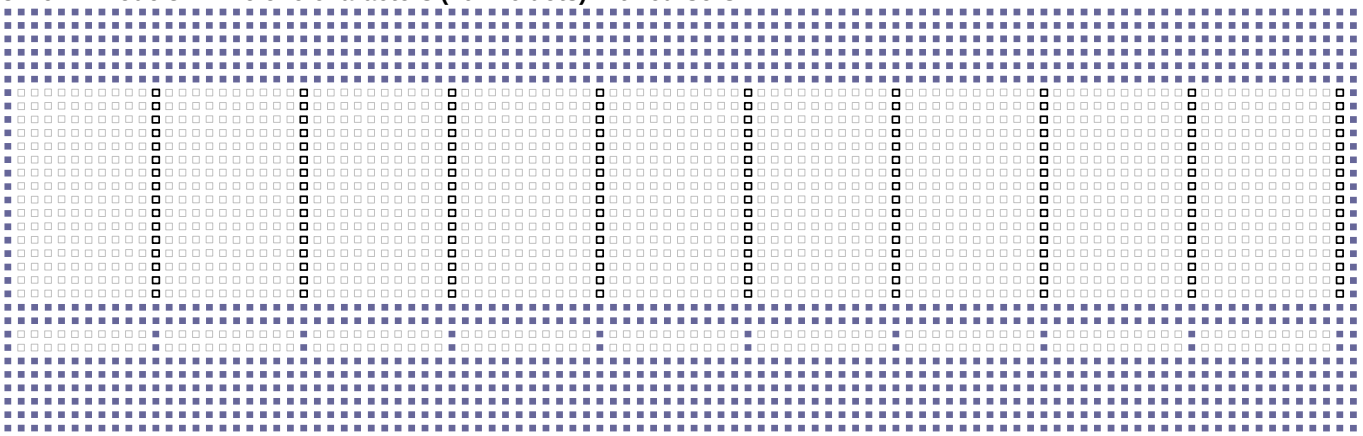


Figure 47 Mode 8 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	1
	Line Start Row	6
	Character Set	3
	Bitmap Width	11
	Bitmap Height	16

Table 83 Mode 8 parameters

8.1.10 Mode 9: 1 line of 9 characters (10x16 dots) with icons

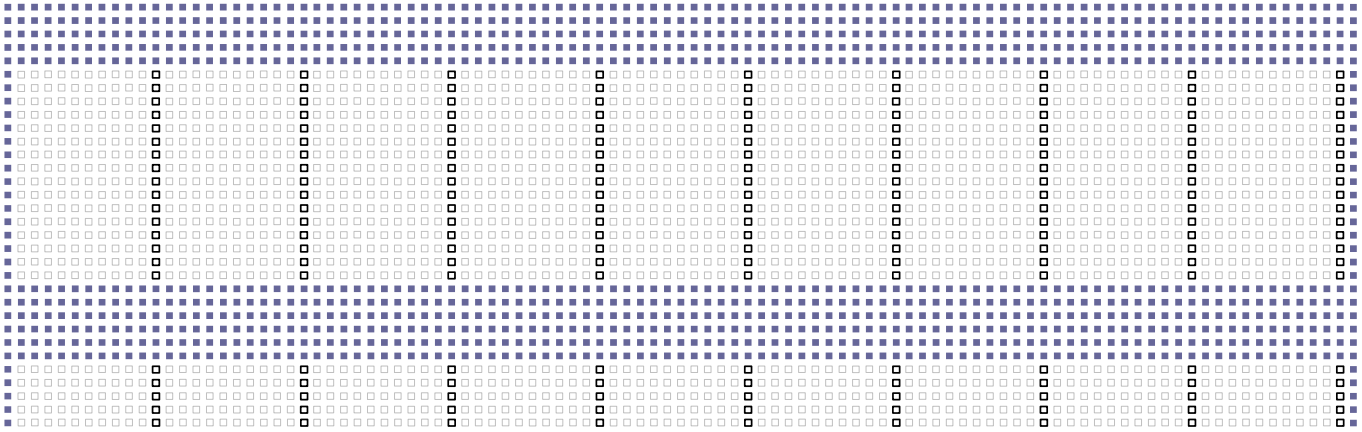


Figure 48 Mode 9 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	1
	Line Start Row	5
	Character Set	3
	Bitmap Width	11
	Bitmap Height	16
2	Line Start Column	1
	Line Start Row	27
	Character Set	3
	Bitmap Width	11
	Bitmap Height	5

Table 84 Mode 9 parameters

8.1.11 Mode 10: 1 line of 16 characters (10 x 16 dots) with icons and cursors

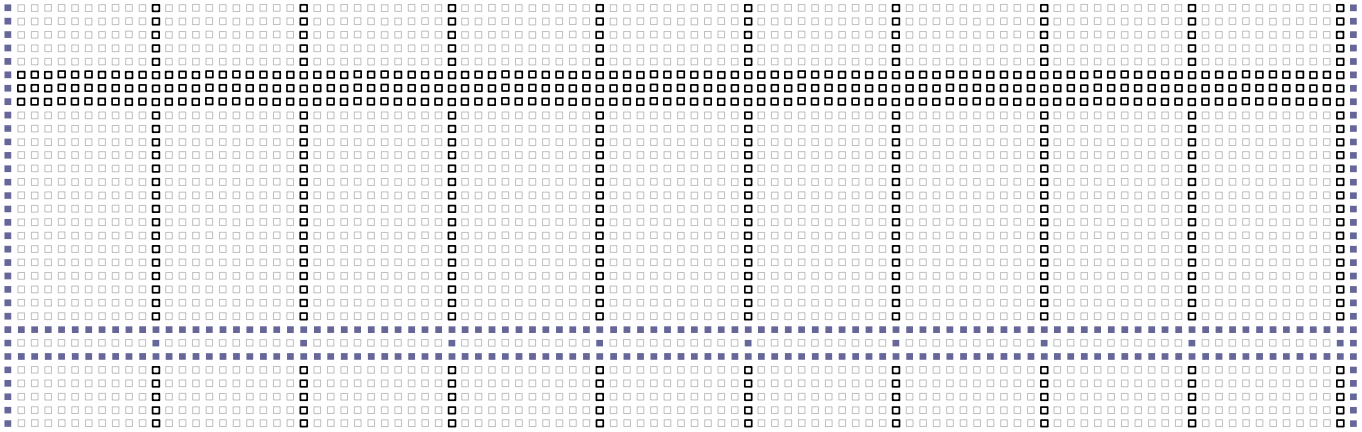


Figure 49 Mode 10 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	1
	Line Start Row	0
	Character Set	3
	Bitmap Width	11
	Bitmap Height	8
2	Line Start Column	1
	Line Start Row	8
	Character Set	3
	Bitmap Width	11
	Bitmap Height	16
3	Line Start Column	1
	Line Start Row	27
	Character Set	3
	Bitmap Width	11
	Bitmap Height	5

Table 85 Mode 10 parameters

8.1.12 Mode 11: 1 line of 16 characters (5 x 10 dots) with icons and cursors

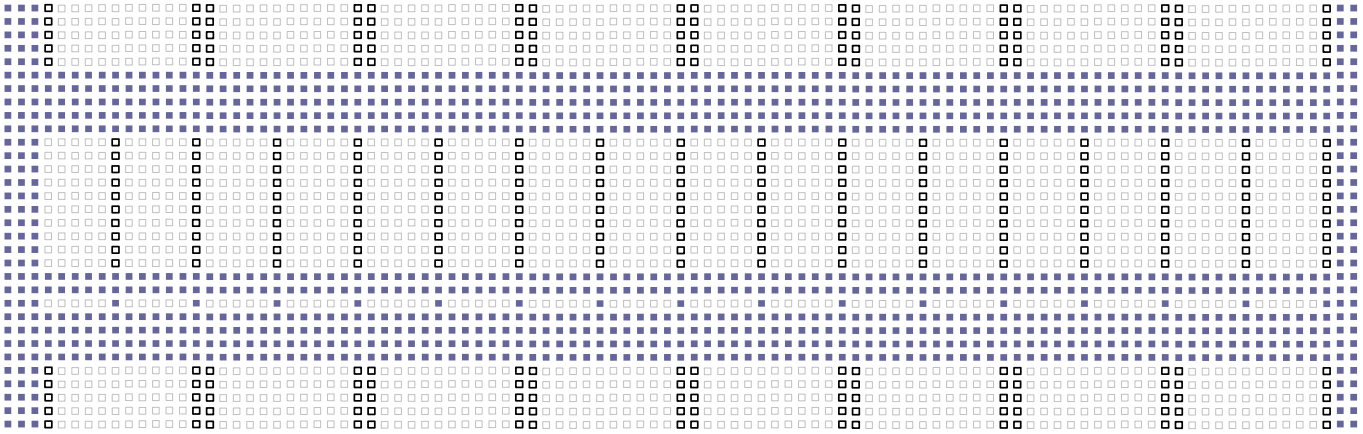


Figure 50 Mode 11 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	3
	Line Start Row	0
	Character Set	3
	Bitmap Width	11
	Bitmap Height	5
2	Line Start Column	3
	Line Start Row	10
	Character Set	2
	Bitmap Width	6
	Bitmap Height	10
3	Line Start Column	3
	Line Start Row	27
	Character Set	3
	Bitmap Width	11
	Bitmap Height	5

Table 86 Mode 11 parameters

8.1.13 Mode 12: 1 line of 17 medium characters (5 x10 dots) and 2 lines of small characters (5x7 dots)

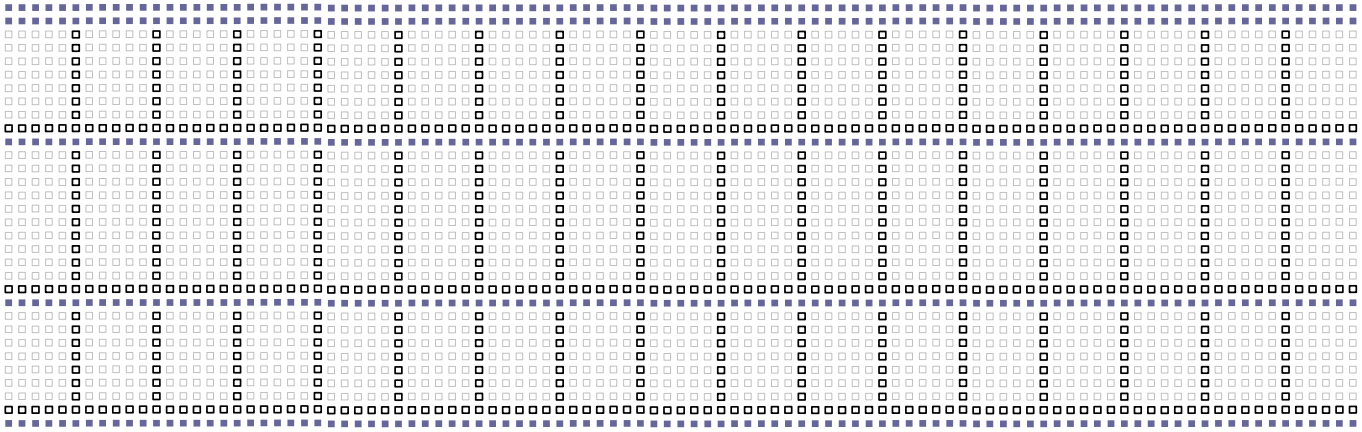


Figure 51 Mode 12 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	2
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8
2	Line Start Column	0
	Line Start Row	11
	Character Set	2
	Bitmap Width	6
	Bitmap Height	11
3	Line Start Column	0
	Line Start Row	23
	Character Set	1
	Bitmap Width	6
	Bitmap Height	8

Table 87 Mode 12 parameters

8.1.14 Mode 13: 1 line of 17 small characters (5 x7 dots) and 1 line of 17 medium characters (5x10 dots) with cursors

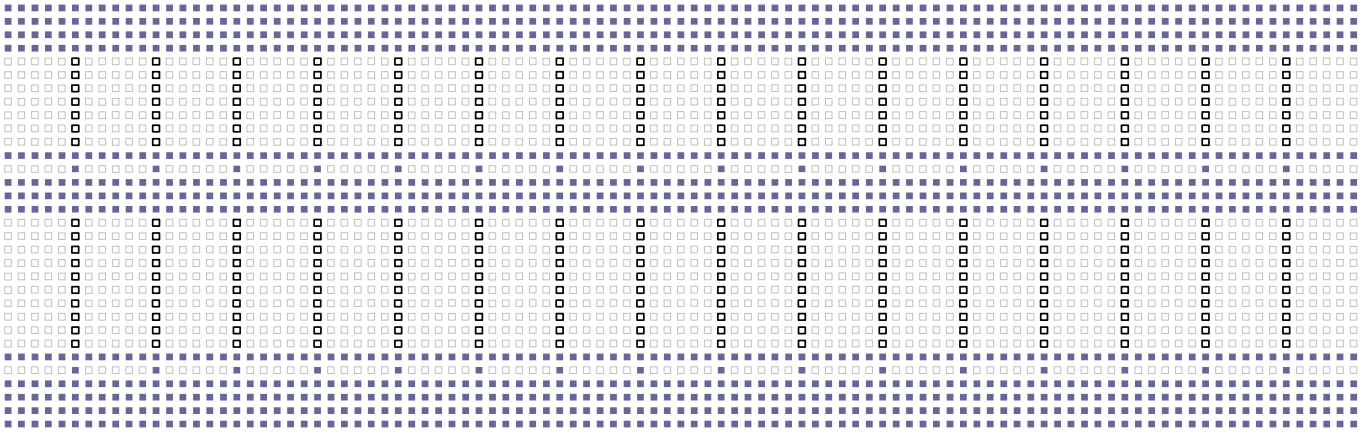


Figure 52 Mode 13 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	4
	Character Set	1
	Bitmap Width	6
	Bitmap Height	7
2	Line Start Column	0
	Line Start Row	16
	Character Set	2
	Bitmap Width	6
	Bitmap Height	10

Table 88 Mode 13 parameters

8.1.15 Mode 14: 1 line of 17 small characters (5 x7 dots)

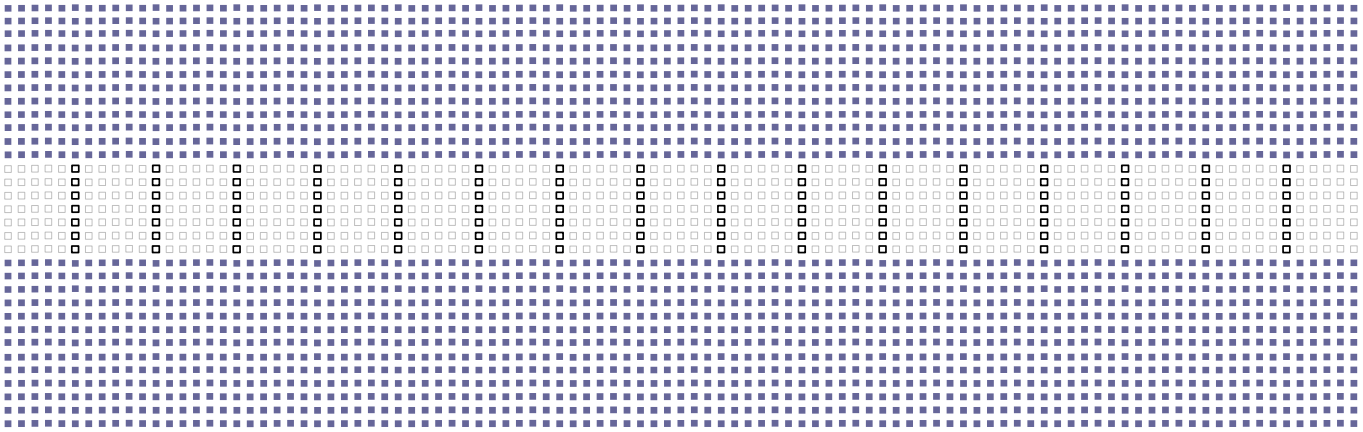


Figure 53 Mode 14 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	0
	Line Start Row	12
	Character Set	1
	Bitmap Width	6
	Bitmap Height	7

Table 89 Mode 14 parameters

8.1.16 Mode 15: 3 lines of 14 small characters (6 x8dots)

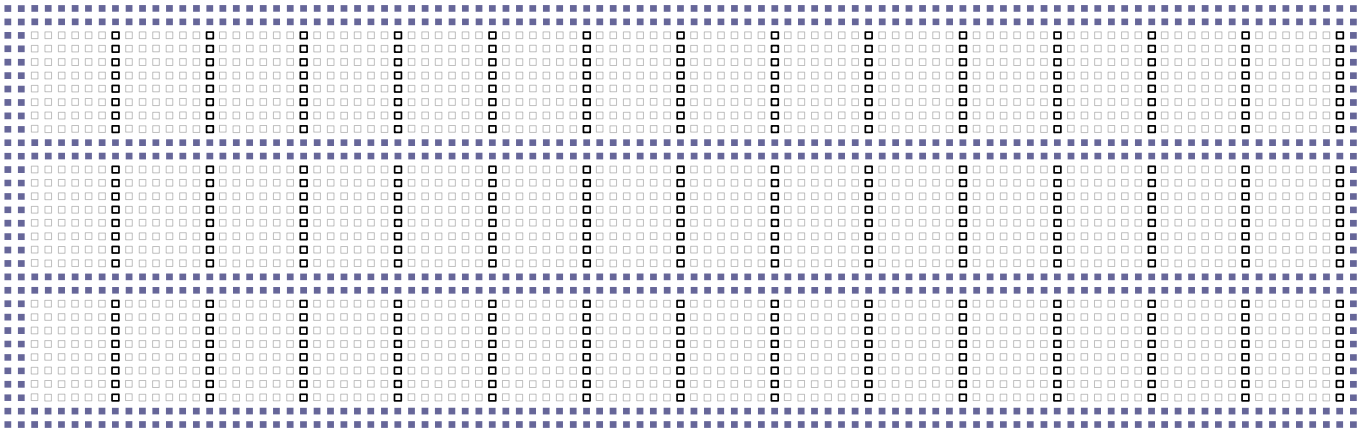


Figure 54 Mode 15 display

Columns number: 101
Rows number: 32

Line	Parameters	Value
1	Line Start Column	2
	Line Start Row	2
	Character Set	0
	Bitmap Width	7
	Bitmap Height	8
2	Line Start Column	12
	Line Start Row	2
	Character Set	0
	Bitmap Width	7
	Bitmap Height	8
3	Line Start Column	22
	Line Start Row	2
	Character Set	0
	Bitmap Width	7
	Bitmap Height	8

Table 90 Mode 15 parameters

8.2 Characters set

8.2.1 5x7 characters

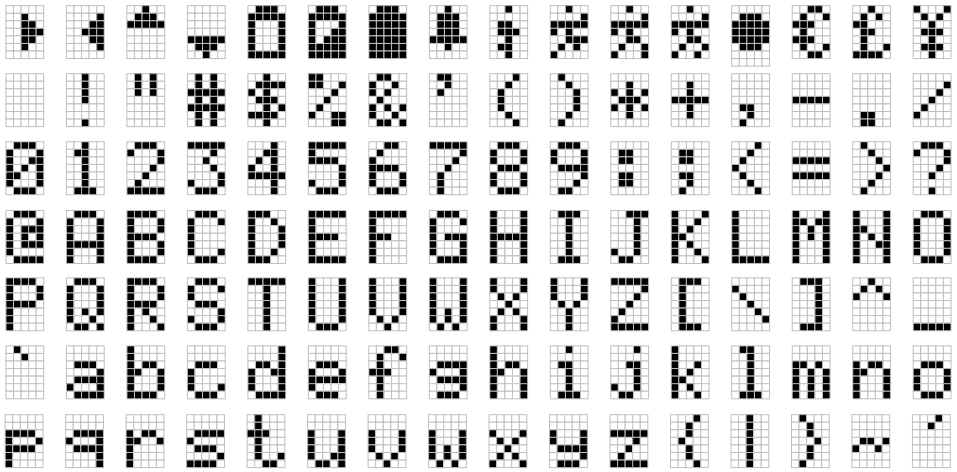


Figure 55 5x7 characters

8.2.2 6x8 characters

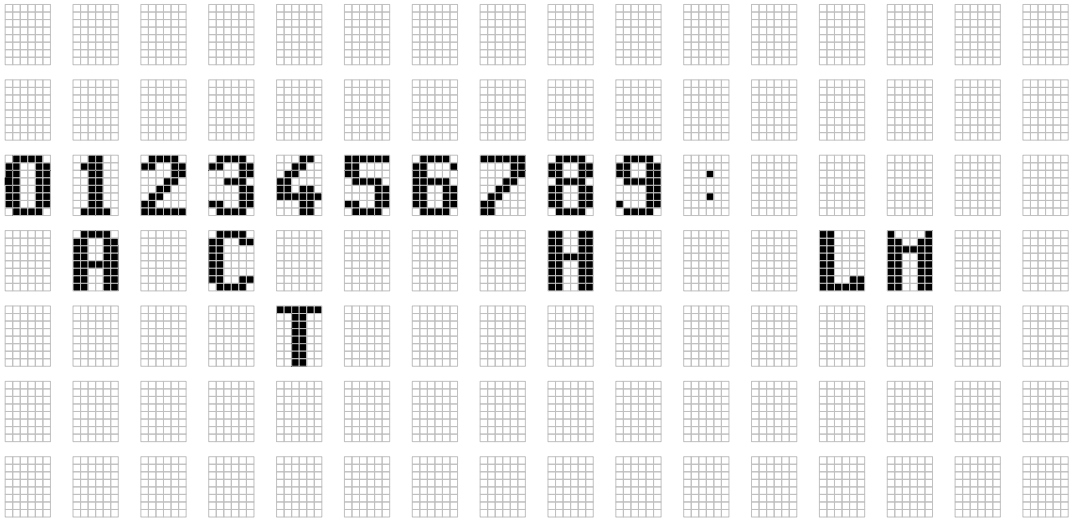


Figure 56 6x8 characters

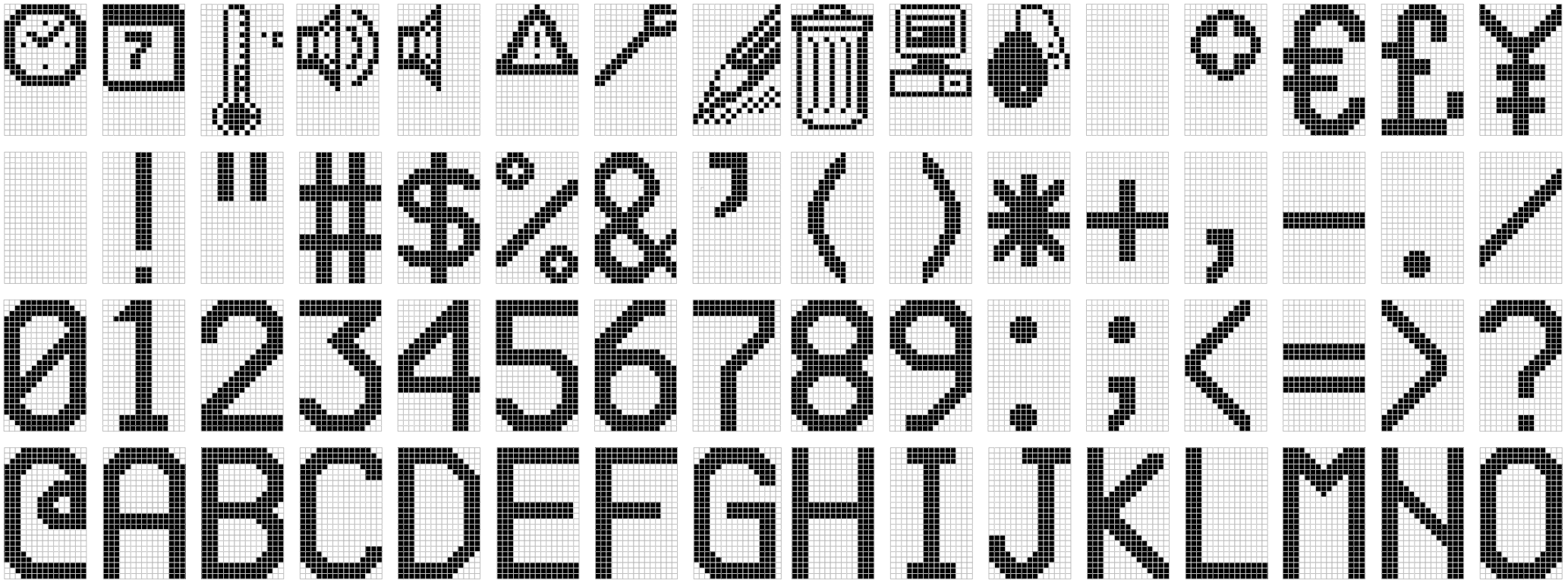
8.2.3 5x10 characters

Figure 57 5x10 characters

8.2.4 10x16 characters

Figure 58 10x 16 characters

8.2.5 15x24 characters



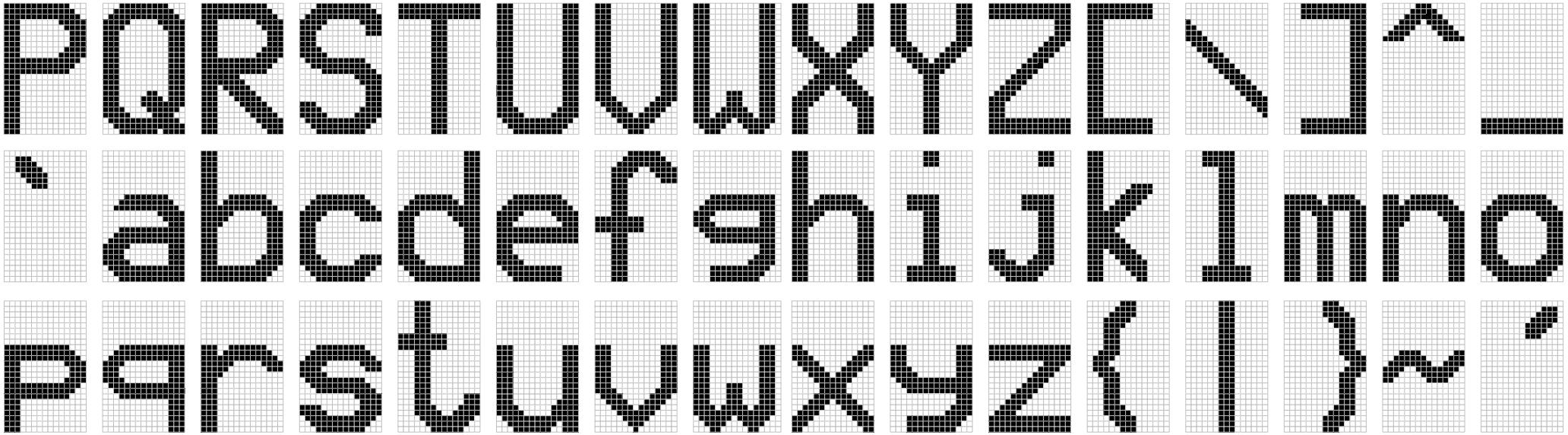


Figure 59 15x24 characters

8.3 ROM Messages

Address	Message
4	TIME
5	ALARM
6	CHRONO
7	SYNCHRO
8	SETTINGS
9	ON
10	OFF
11	AM
12	PM
13	METEO
14	ALTIMETER
15	THERMO
16	COMPASS
17	CALIBRATION
18	MON
19	TUE
20	WED
21	THU
22	FRI
23	SAT
24	SUN
25	JAN
26	FEB
27	MAR
28	APR
29	MAY
30	JUN
31	JUL
32	AUG
33	SEP
34	OCT
35	NOV
36	DEC
37	PLEASE WAIT
38	BOOTING
39	CALIBRATING
40	Asulab
41	A division of
42	The Swatch Group RD Ltd
43	The Swatch Group
44	Research and Development Ltd
45	EM6127
46	LCD and LED driver
47	Programmable font format
48	bitmap mode
49	16 predefined modes
50	Horizontal, vertical scrolling
51	Full and partial
52	Reverse display
53	Inverse
54	Blink
55	Cursor
56	Character superposition
57	4 sequences
58	One character line mode

Table 91 Predefined messages table

9 BUMP LOCATION DIAGRAM

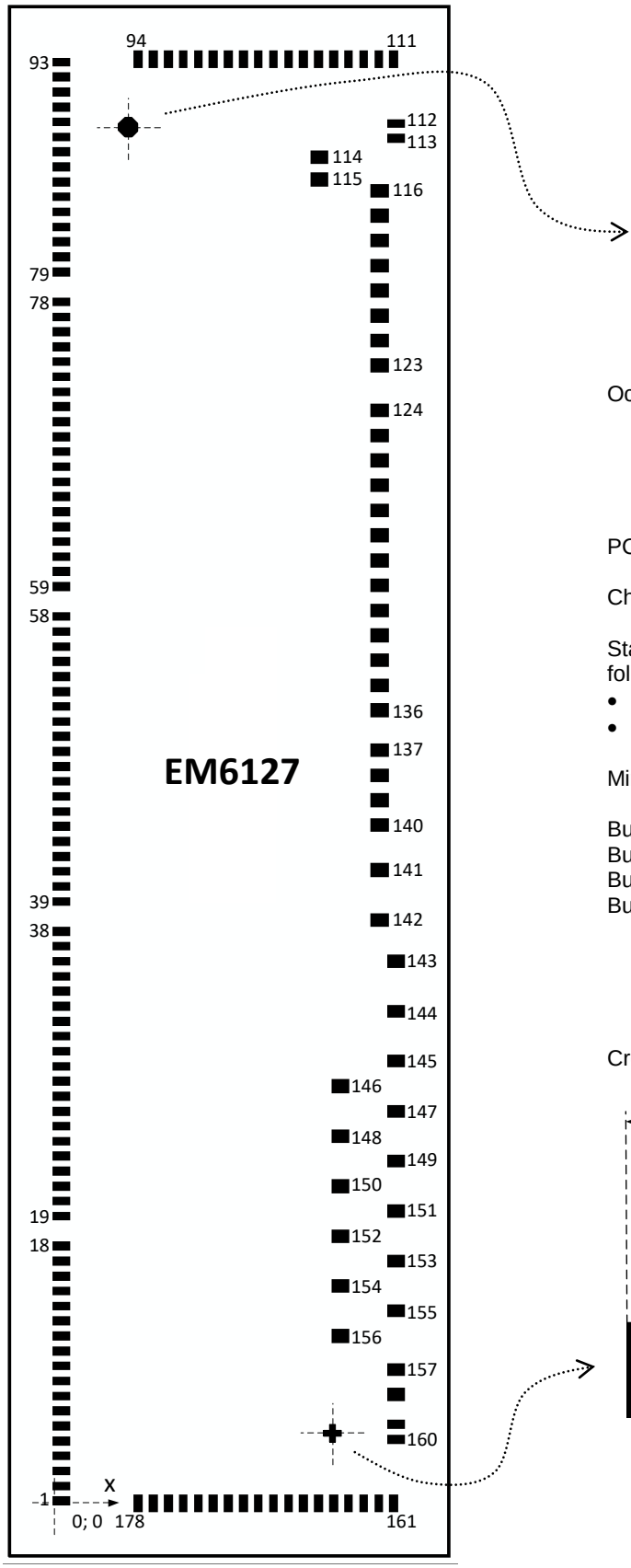
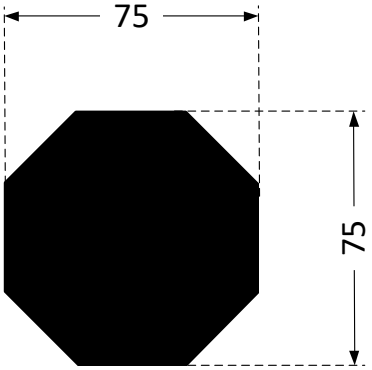


Figure 60: IC Bump View



Octogone centre: X=263.34 µm; Y=5518.34 µm

PCB view is mirror of this Bump View

Chip size: 1531 µm x 5976 µm.

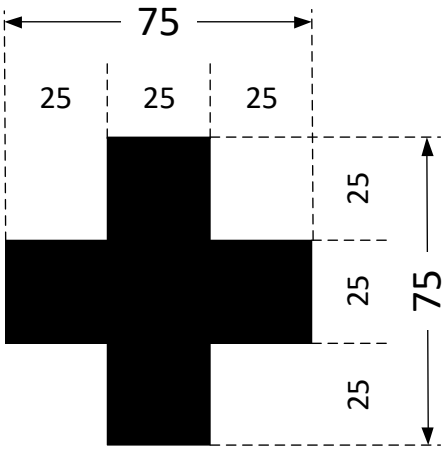
Standard delivery includes gold bumps on all bumps with following dimensions:

- 80 µm x 40 µm: 133 LCD bumps (rows, columns)
- 80 µm x 60 µm: 45 communication, other bumps

Minimum bumps pitch is 60 µm.

Bump to scribe RIGHT:	57.16 microns
Bump to scribe LEFT:	57.16 microns
Bump to scribe TOP:	57.16 microns
Bump to scribe BOTTOM:	57.16 microns

Cross centre: X=1073.34 µm; Y=268.34 µm



Bumps located on LEFT side:			Bumps located on RIGHT side:		
1	pc<4>	X=0.00; Y= 10.84	112	pr<3>	X=1336.68; Y=5524.84
2	pc<5>	X=0.00; Y= 70.84	113	pr<1>	X=1336.68; Y=5464.84
3	pc<6>	X=0.00; Y=130.84	114	rfu1	X=1030.06; Y=5389.84
4	pc<7>	X=0.00; Y=190.84	115	rfu2	X=1030.06; Y=5299.84
5	pc<8>	X=0.00; Y=250.84	116	pirq	X=1270.06; Y=5255.84
6	pc<9>	X=0.00; Y=310.84	117	pcio0	X=1270.06; Y=5155.84
7	pc<10>	X=0.00; Y=370.84	118	pcio1	X=1270.06; Y=5055.84
8	pc<11>	X=0.00; Y=430.84	119	pcio2	X=1270.06; Y=4955.84
9	pc<12>	X=0.00; Y=490.84	120	pci3	X=1270.06; Y=4855.84
10	pc<13>	X=0.00; Y=550.84	121	pcio4	X=1270.06; Y=4755.84
11	pc<14>	X=0.00; Y=610.84	122	pclk	X=1270.06; Y=4655.84
12	pc<15>	X=0.00; Y=670.84	123	vssa	X=1270.06; Y=4555.84
13	pc<16>	X=0.00; Y=730.84	124	vssd	X=1270.06; Y=4375.84
14	pc<17>	X=0.00; Y=790.84	125	plsv	X=1270.06; Y=4275.84
15	pc<18>	X=0.00; Y=850.84	126	pcis	X=1270.06; Y=4175.84
16	pc<19>	X=0.00; Y=910.84	127	pci5	X=1270.06; Y=4075.84
17	pc<20>	X=0.00; Y=970.84	128	vddd	X=1270.06; Y=3975.84
18	pc<21>	X=0.00; Y=1030.84	129	pn_rst	X=1270.06; Y=3875.84
19	pc<22>	X=0.00; Y=1150.84	130	pen	X=1270.06; Y=3775.84
20	pc<23>	X=0.00; Y=1210.84	131	pfr	X=1270.06; Y=3675.84
21	pc<24>	X=0.00; Y=1270.84	132	pci6	X=1270.06; Y=3575.84
22	pc<25>	X=0.00; Y=1330.84	133	pci7	X=1270.06; Y=3475.84
23	pc<26>	X=0.00; Y=1390.84	134	pci8	X=1270.06; Y=3375.84
24	pc<27>	X=0.00; Y=1450.84	135	vdd	X=1270.06; Y=3275.84
25	pc<28>	X=0.00; Y=1510.84	136	pvddc	X=1270.06; Y=3175.84
26	pc<29>	X=0.00; Y=1570.84	137	pvdda	X=1270.06; Y=3015.84
27	pc<30>	X=0.00; Y=1630.84	138	pvcp	X=1270.06; Y=2915.84
28	pc<31>	X=0.00; Y=1690.84	139	pcbl	X=1270.06; Y=2815.84
29	pc<32>	X=0.00; Y=1750.84	140	pcbh	X=1270.06; Y=2715.84
30	pc<33>	X=0.00; Y=1810.84	141	vssp	X=1270.06; Y=2535.84
31	pc<34>	X=0.00; Y=1870.84	142	vssp	X=1270.06; Y=2335.84
32	pc<35>	X=0.00; Y=1930.84	143	pcp2h	X=1336.68; Y=2170.84
33	pc<36>	X=0.00; Y=1990.84	144	pcp2l	X=1336.68; Y=1970.84
34	pc<37>	X=0.00; Y=2050.84	145	pcp1h	X=1336.68; Y=1770.84
35	pc<38>	X=0.00; Y=2110.84	146	psw1	X=1114.06; Y=1670.84
36	pc<39>	X=0.00; Y=2170.84	147	pcp1l	X=1336.68; Y=1570.84
37	pc<40>	X=0.00; Y=2230.84	148	psw0	X=1114.06; Y=1470.84
38	pc<41>	X=0.00; Y=2290.84	149	pcp3h	X=1336.68; Y=1370.84
39	pc<42>	X=0.00; Y=2410.84	150	pvled1	X=1114.06; Y=1270.84
40	pc<43>	X=0.00; Y=2470.84	151	pcp3l	X=1336.68; Y=1170.84
41	pc<44>	X=0.00; Y=2530.84	152	pvled0	X=1114.06; Y=1070.84
42	pc<45>	X=0.00; Y=2590.84	153	pcp4h	X=1336.68; Y=970.84
43	pc<46>	X=0.00; Y=2650.84	154	ppwm2	X=1114.06; Y=870.84
44	pc<47>	X=0.00; Y=2710.84	155	pcp4l	X=1336.68; Y=770.84
45	pc<48>	X=0.00; Y=2770.84	156	ppwm1	X=1114.06; Y=670.84
46	pc<49>	X=0.00; Y=2830.84	157	pvlcd_out	X=1336.68; Y=536.84
47	pc<50>	X=0.00; Y=2890.84	158	pvlcd_in	X=1336.68; Y=436.84
48	pc<51>	X=0.00; Y=2950.84	159	pr<0>	X=1336.68; Y=316.84
49	pc<52>	X=0.00; Y=3010.84	160	pr<2>	X=1336.68; Y=256.84
50	pc<53>	X=0.00; Y=3070.84			
51	pc<54>	X=0.00; Y=3130.84			
52	pc<55>	X=0.00; Y=3190.84			
53	pc<56>	X=0.00; Y=3250.84			
54	pc<57>	X=0.00; Y=3310.84			
55	pc<58>	X=0.00; Y=3370.84			
56	pc<59>	X=0.00; Y=3430.84			
57	pc<60>	X=0.00; Y=3490.84			
58	pc<61>	X=0.00; Y=3550.84			
59	pc<62>	X=0.00; Y=3670.84			
60	pc<63>	X=0.00; Y=3730.84			
61	pc<64>	X=0.00; Y=3790.84			

62 pc<65> X=0.00; Y=3850.84 63 pc<66> X=0.00; Y=3910.84 64 pc<67> X=0.00; Y=3970.84 65 pc<68> X=0.00; Y=4030.84 66 pc<69> X=0.00; Y=4090.84 67 pc<70> X=0.00; Y=4150.84 68 pc<71> X=0.00; Y=4210.84 69 pc<72> X=0.00; Y=4270.84 70 pc<73> X=0.00; Y=4330.84 71 pc<74> X=0.00; Y=4390.84 72 pc<75> X=0.00; Y=4450.84 73 pc<76> X=0.00; Y=4510.84 74 pc<77> X=0.00; Y=4570.84 75 pc<78> X=0.00; Y=4630.84 76 pc<79> X=0.00; Y=4690.84 77 pc<80> X=0.00; Y=4750.84 78 pc<81> X=0.00; Y=4810.84 79 pc<82> X=0.00; Y=4930.84 80 pc<83> X=0.00; Y=4990.84 81 pc<84> X=0.00; Y=5050.84 82 pc<85> X=0.00; Y=5110.84 83 pc<86> X=0.00; Y=5170.84 84 pc<87> X=0.00; Y=5230.84 85 pc<88> X=0.00; Y=5290.84 86 pc<89> X=0.00; Y=5350.84 87 pc<90> X=0.00; Y=5410.84 88 pc<91> X=0.00; Y=5470.84 89 pc<92> X=0.00; Y=5530.84 90 pc<93> X=0.00; Y=5590.84 91 pc<94> X=0.00; Y=5650.84 92 pc<95> X=0.00; Y=5710.84 93 pc<96> X=0.00; Y=5770.84	
Bumps located on TOP side: 94 pc<97> X= 305.84; Y=5781.68 95 pc<98> X= 365.84; Y=5781.68 96 pc<99> X= 425.84; Y=5781.68 97 pc<100>X= 485.84; Y=5781.68 98 pr<31> X= 545.84; Y=5781.68 99 pr<29> X= 605.84; Y=5781.68 100 pr<27> X= 665.84; Y=5781.68 101 pr<25> X= 725.84; Y=5781.68 102 pr<23> X= 785.84; Y=5781.68 103 pr<21> X= 845.84; Y=5781.68 104 pr<19> X= 905.84; Y=5781.68 105 pr<17> X= 965.84; Y=5781.68 106 pr<15> X=1025.84; Y=5781.68 107 pr<13> X=1085.84; Y=5781.68 108 pr<11> X=1145.84; Y=5781.68 109 pr<9> X=1205.84; Y=5781.68 110 pr<7> X=1265.84; Y=5781.68 111 pr<5> X=1325.84; Y=5781.68	**Bumps located on BOTTOM side:** 161 pr<4> X=1325.84; Y=0.00 162 pr<6> X=1265.84; Y=0.00 163 pr<8> X=1205.84; Y=0.00 164 pr<10> X=1145.84; Y=0.00 165 pr<12> X=1085.84; Y=0.00 166 pr<14> X=1025.84; Y=0.00 167 pr<16> X= 965.84; Y=0.00 168 pr<18> X= 905.84; Y=0.00 169 pr<20> X= 845.84; Y=0.00 170 pr<22> X= 785.84; Y=0.00 171 pr<24> X= 725.84; Y=0.00 172 pr<26> X= 665.84; Y=0.00 173 pr<28> X= 605.84; Y=0.00 174 pr<30> X= 545.84; Y=0.00 175 pc<0> X= 485.84; Y=0.00 176 pc<1> X= 425.84; Y=0.00 177 pc<2> X= 365.84; Y=0.00 178 pc<3> X= 305.84; Y=0.00

Total Bumps Number: 178 Coordinate unit: Micron
Notes: X,Y are the coordinates of Bump center.

10 VERSIONS AND ORDERING INFORMATION

A single version if the EM6127 is available

Ordering code	Description	Packaging	Container
EM6127V01WP8E	Ultra Low Power LCD Driver with Character Generator Memories	Bare die with Gold bumps	Waffle Pack