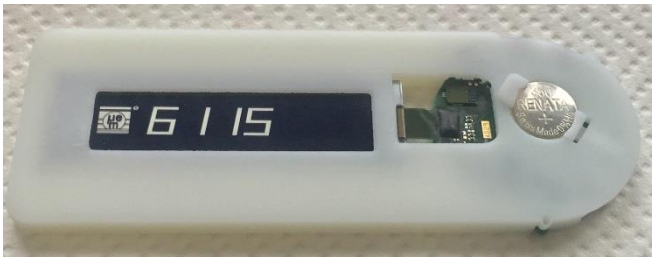


# Extreme Low Power LCD Driver

## GENERAL DESCRIPTION

The device EM6115 is an extremely flexible, ultra-low power and low voltage LCD segment driver supporting static, Mux2, Mux3 and Mux4 addressing with ½ and ⅓ biasing.

The internally generated LCD voltage levels assure a stable display contrast over the full IC supply range.

The internal segment-mapping directory allows display updates with minimal energy by keeping the serial data transfer at a strict minimum.

## APPLICATIONS

- Portable, battery operated devices
- Wearables
- IoT devices
- Decentralized sensors
- Always-on Displays
- Weight scales, utility meters
- Home appliances

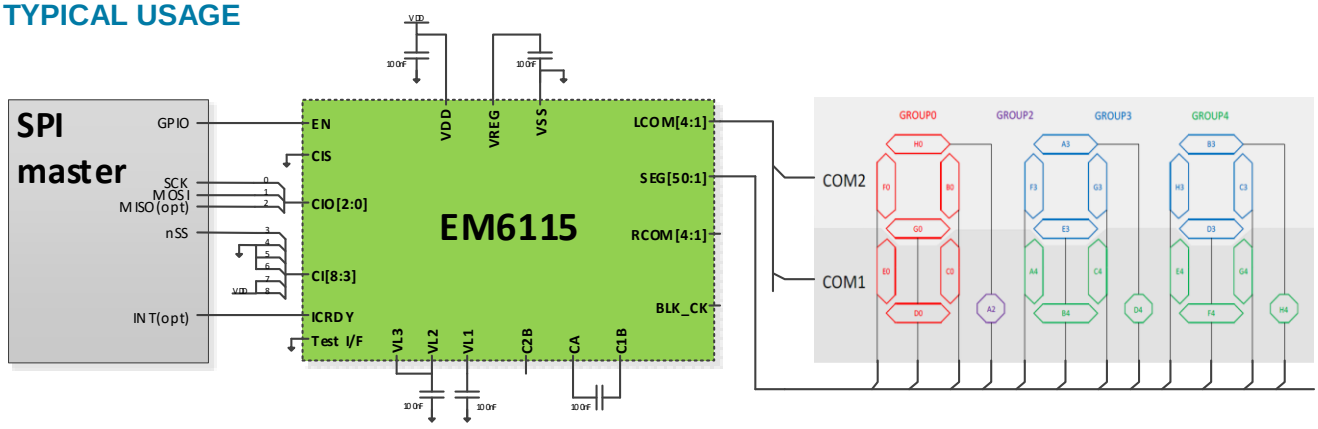
## AVAILIBILITY

- Naked die (for wirebonding assembly)
- Gold Bump for COG, COF
- Others, please contact EM-Microelectronic-Marin

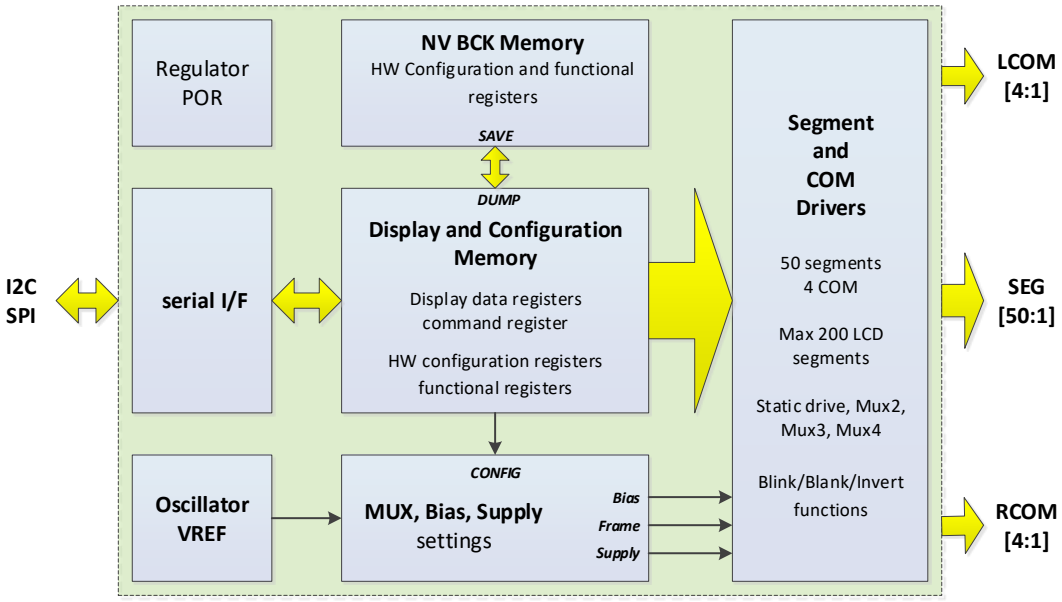
## FEATURES

- Up to **50 SEG and 4 COM** physical lines, for a maximum of 200 physical segments.
- For easier connection COM lines are provided on each side of the SEG lines (LCOM and RCOM).
- The unused SEG and COM outputs can be disabled
- Control of the LCD segments by 32 groups of logical segments (up to 8 bits each), configurable with a mapping dictionary.
- Internal E²PROM for automatic configuration of operating parameters and segment mapping dictionary after reset or power-up.
- Supported Mux rates: **Static, Mux2, Mux3, Mux4**
- Mux2, Mux3, Mux4 can use either ½ or ⅓ biasing.
- On-Chip generation of the LCD waveform and frame frequency.
- **On-Chip programmable voltage reference** for the LCD Bias voltage generation (25mV steps).
- Selectable **I²C** or **SPI** interface
- Selectable blink behavior (global or segment-defined blink) and blink frequency
- Blank function and Inverse function available
- **Wide voltage range** from 1 V to 3.6 V range
- **Ultra-low power operation**: 130 nA (at 3 V, Mux2, bias ½ and without LCD)
- **EN pin**, Switch-off mode below 10nA
- Temperature range: -40°C to +85°

## TYPICAL USAGE



## SIMPLIFIED BLOCKDIAGRAM



# EM6115 DATASHEET

## Table of Contents

# 1. PRODUCT DESCRIPTION

The device EM6115 is an extremely low power and low voltage LCD segment driver. The circuit includes an on-chip LCD supply voltages generator and supports static, Mux2, Mux3 and Mux4 addressing with ½ and ⅓ biasing. The internal voltage reference is adjustable in 25mV steps.

A maximum of 200 display segments can be addressed using the 50 segment lines (SEG) and the four common lines (COM). Host data interface uses either simplified I2C or SPI protocol.

To simplify the PCB all common lines are provided on the left AND the right side of the circuit. Unused COM and SEG outputs can individually be disabled to save power.

## 1.1. OPERATING MODES

An internal mapping directory allows easy segment grouping (32 groups of max 8 segments each). This mapping greatly reduces the complexity of the display update firmware as well as the necessary data transfer length.

Global BLINK, BLANK and INVERSE display function as well as individual BLINK bits are implemented to further reduce the display driver firmware complexity.

The internal E2PROM holds all configuration data, the operating parameters and the display mapping directory. At circuit start-up, these data are automatically copied into the local registers. Any configuration change can easily be saved in the E2PROM (Dump command).

While the EN pin is at low level, the EM6115 internal power is fully switched off while maintaining the selected $I^2C$ pull-up resistors. In this mode, the circuit consumes less than 10nA.

### 1.1.1. BLOCK DIAGRAM

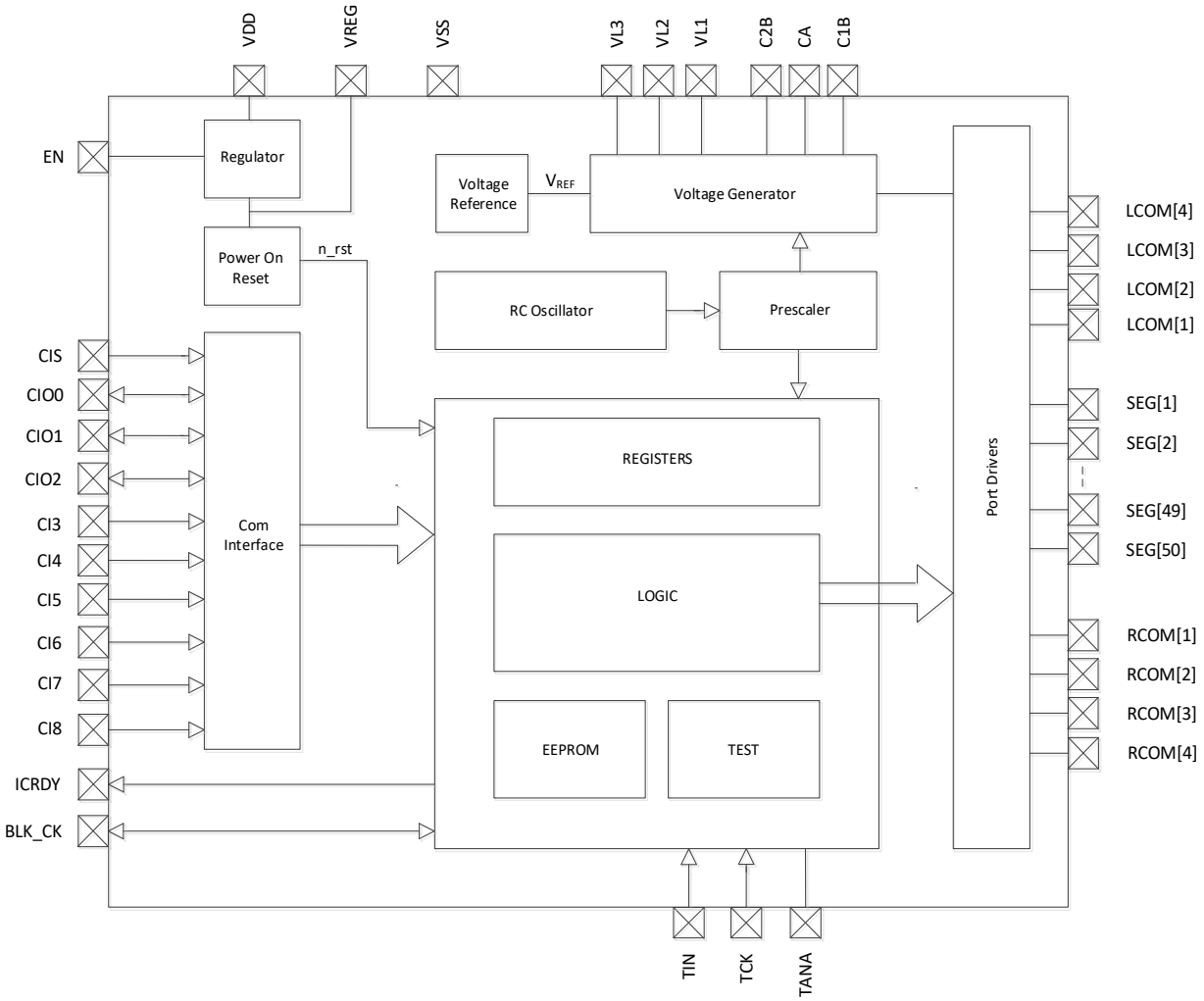



**Figure 1-1 : Block diagram**

## 1.2. PIN DESCRIPTION

| # | Name | Type | Description | Remark |
|---|---|---|---|---|
| 73 | **VDD** | P | Power supply voltage input | |
| 72 | **VSS** | P | Ground | |
| 71 | **VREG** | P | Regulated voltage for digital part | Internal use only |
| 57 | **EN** | I | Device enable | It should not be left floating |
| 56 | **ICRDY** | O | Device ready signal | See Note [1] |
| 58 | **CIS** | I | I²C/SPI COMM interface selection | See Note [2] |
| 59 | **CIO0/SCL/SCK** | I/O | I²C Clock or SPI Clock | It should not be left floating |
| 60 | **CIO1/SDA/MOSI** | I/O | I²C Data or SPI Data In | It should not be left floating |
| 61 | **CIO2/EN_IWPU/MISO** | I/O | Enable I²C internal Weak Pull-Up resistors or SPI data Output | See Note [3] |
| 62 | **CI3/EN_ISPU/nSS** | I | Enable I²C internal Strong Pull-Up resistors or SPI Slave Select (active low) | It should not be left floating |
| 63 | **CI4/A0** | I | I²C address bit 0 | It should not be left floating |
| 64 | **CI5/A1/CK_POL** | I | I²C address bit 1 or SPI SCK Polarity | It should not be left floating |
| 65 | **CI6/A2/CK_PHA** | I | I²C address bit 2 or SPI SCK Phase | It should not be left floating |
| 66 | **CI7/A3/MSB_FIRST** | I | I²C address bit 3 or SPI MSB First selection | It should not be left floating |
| 67 | **CI8/ICRDY_POL** | I | ICRDY polarity | It should not be left floating |
| 55 | **BLK_CK** | I/O | Blink synchronization clock | See Note [4] |
| 69 | **TIN** | I | Test mode input | Internal pulldown. Connect to VSS |
| 68 | **TCK** | I | Test Clock input | Internal pulldown. Connect to VSS |
| 70 | **TANA** | A | Analog test port | Internal pulldown. Connect to VSS |
| 75 | **CA** | A | External capacitor connector for charge pumps 1 & 2 | |
| 76 | **C1B** | A | External capacitor connector for charge pump 1 | |
| 74 | **C2B** | A | External capacitor connector for charge pump 2 | |
| 79 | **VL1** | P | LCD power supply voltage | |
| 78 | **VL2** | P | LCD power supply voltage | |
| 77 | **VL3** | P | LCD power supply voltage | |
| 51-54 | **RCOM[4:1]** | O | Bus of COM lines located at the right of the SEG lines | They can be individually disabled |
| 80-83 | **LCOM[4:1]** | O | Bus of COM lines located at the left of the SEG lines | They can be individually disabled |
| 1-50 | **SEG[50:1]** | O | Bus of SEG lines | They can be individually disabled |

| Pin type | Description |
|---|---|
| P | Power supply |
| A | Analog |
| I | Input |
| O | Output |
| I/O | Depending on the selected configuration (Bidir, Input, Output, Open-Drain) |

[1] When it is active means that the start-up of the device is finished and it is ready to receive commands.
[2] It should not be left floating. When the pin is connected to VDD, the I²C interface is selected. When it is connected to VSS, the SPI interface is selected.
[3] It should not be left floating. In SPI, the pin can be disabled through the bit “en_MISO” in the configuration registers.
[4] It can be enabled by the bit “Blk_Share” in the configuration registers. When enabled it is either a push-pull output or an input without pulldown. When disabled or when EN = VSS, there is an internal pulldown. If it is never used, it should be connected to VSS.

# 2. FUNCTIONAL DESCRIPTION

## 2.1. LCD ADRESSING

The LCD driver generates all necessary voltages and output signals to drive an LCD with different multiplex and bias schemes. The frame frequency is programmable, a lower frequency implies a lower consumption.

In a segment LCD, the backplanes are connected to COM lines and the electrodes are connected to SEG lines. In static addressing, one SEG line drives one LCD segment, in Mux2 it drives two, in Mux3 it drives three and in Mux4 it drives four. Therefore, static addressing needs one COM line, Mux2 needs two, Mux3 needs three and Mux4 needs four. The maximum number of addressable LCD segments as a function of the multiplex rate is:

- Static: 50 LCD segments
- Mux2: 100 LCD segments
- Mux3: 150 LCD segments
- Mux4: 200 LCD segments

The voltage difference between SEG line and COM line is the voltage across the LCD segment. This voltage has a square-wave-like waveform, its root mean square (RMS) value determines whether the segment is ON or OFF. During LCD operation, the average voltage across any LCD segment must be zero.

In Mux2, Mux3 and Mux4 two bias schemes can be chosen: ½ and ⅓. Bias ½ uses voltages VL1 and VL2. Bias ⅓ uses VL1, VL2 and VL3. In terms of power consumption, bias ½ is recommended. In Mux3 and Mux4, bias ⅓ has a bigger contrast ($V_{ON}/V_{OFF}$).

For VDD ≥ 1.68 V, a special low power mode is available in Mux2, Mux3 and Mux4 which reduces the overall power consumption of the LCD driver and the display. For additional information see the subsection 2.1.5.

Considering that: $VL2 = 2\,x\,VL1$ and $VL3 = 3\,x\,VL1$; the RMS voltages of the $V_{ON}$ and $V_{OFF}$ LCD waveforms are shown in the following table.

| | Bias | $V_{ON}$ | $V_{OFF}$ |
|---|---|---|---|
| **Static** | | $V_{REF}/2\,, V_{REF}, 2\,x\,V_{REF}$ *or* $3\,x\,V_{REF}$ | 0 |
| **Mux2** | $^1/_2$ | $\sqrt{\frac{VL1^2 + VL2^2}{2}} = 1.581 \cdot VL1$ | $\sqrt{\frac{1}{2}} \cdot VL1 = 0.707 \cdot VL1$ |
| | $^1/_3$ | $\sqrt{\frac{VL1^2 + VL3^2}{2}} = 2.236 \cdot VL1$ | $VL1$ |
| **Mux3** | $^1/_2$ | $\sqrt{\frac{2 \cdot VL1^2 + VL2^2}{3}} = 1.414 \cdot VL1$ | $\sqrt{\frac{2}{3}} \cdot VL1 = 0.816 \cdot VL1$ |
| | $^1/_3$ | $\sqrt{\frac{2 \cdot VL1^2 + VL3^2}{3}} = 1.915 \cdot VL1$ | $VL1$ |
| **Mux4** | $^1/_2$ | $\sqrt{\frac{3 \cdot VL1^2 + VL2^2}{4}} = 1.323 \cdot VL1$ | $\sqrt{\frac{3}{4}} \cdot VL1 = 0.866 \cdot VL1$ |
| | $^1/_3$ | $\sqrt{\frac{3 \cdot VL1^2 + VL3^2}{4}} = 1.732 \cdot VL1$ | $VL1$ |

**Table 2-1 : $V_{ON}$ and $V_{OFF}$ as a function of Mux and Bias**

In static addressing all the 4 COM lines drive the same backplane signal, they can be connected together externally if high output drive is needed. In Mux2 addressing COM1 and COM3 drive the same signal, the same happens for COM2 and COM4. The COM lines can be disabled if they are not used, in that case they output VSS.

A set of COM lines is provided at each side of the SEG lines (LCOM and RCOM) to increase flexibility of LCD layout and connectivity between the LCD driver and the display.

## 2.1.1. LCD WAVEFORMS

### 2.1.1.1. STATIC MODE

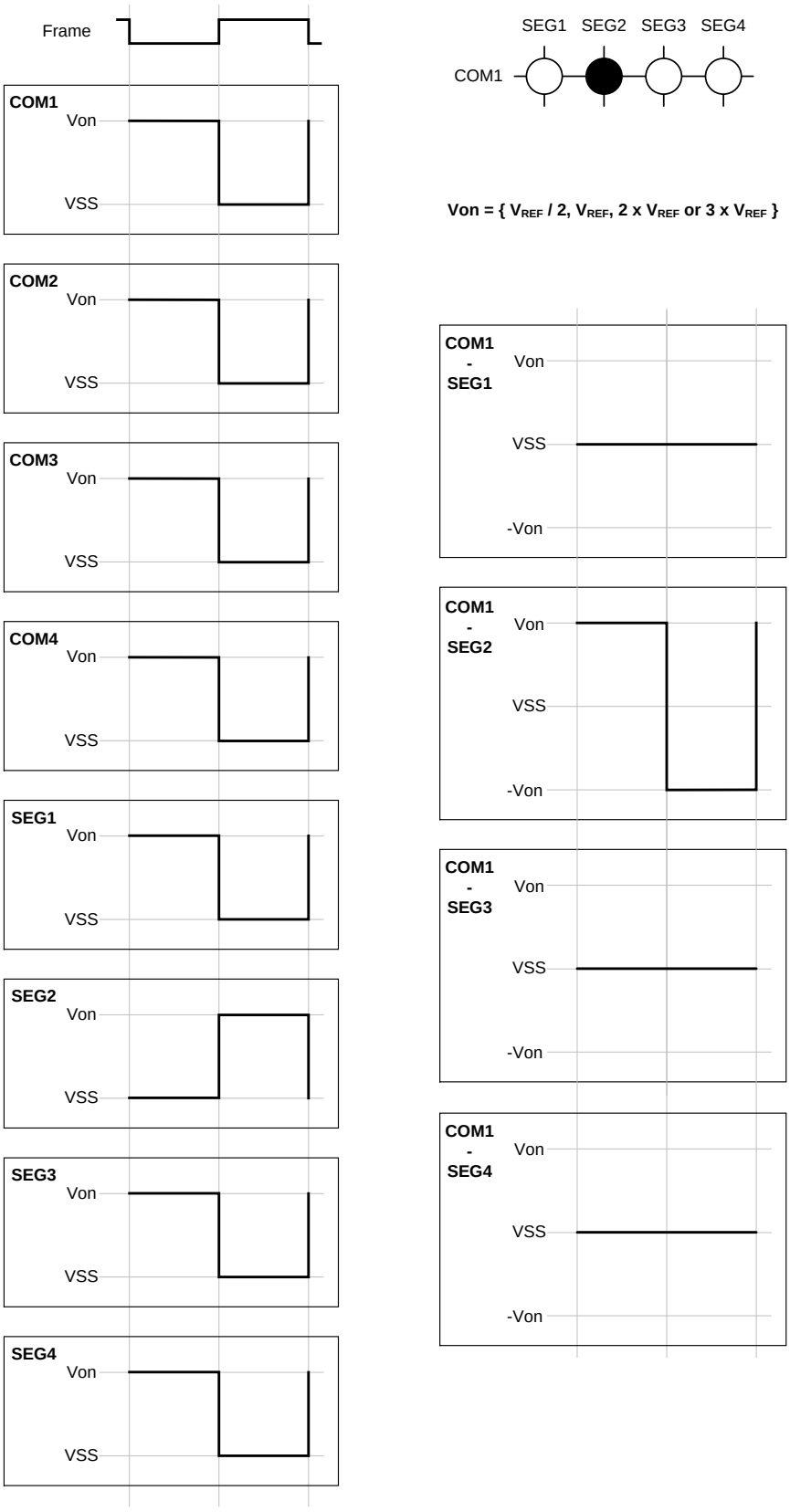



**Figure 2-1 : LCD Driver Waveforms – Static mode**

### 2.1.1.2. MUX2 & BIAS ½ MODE

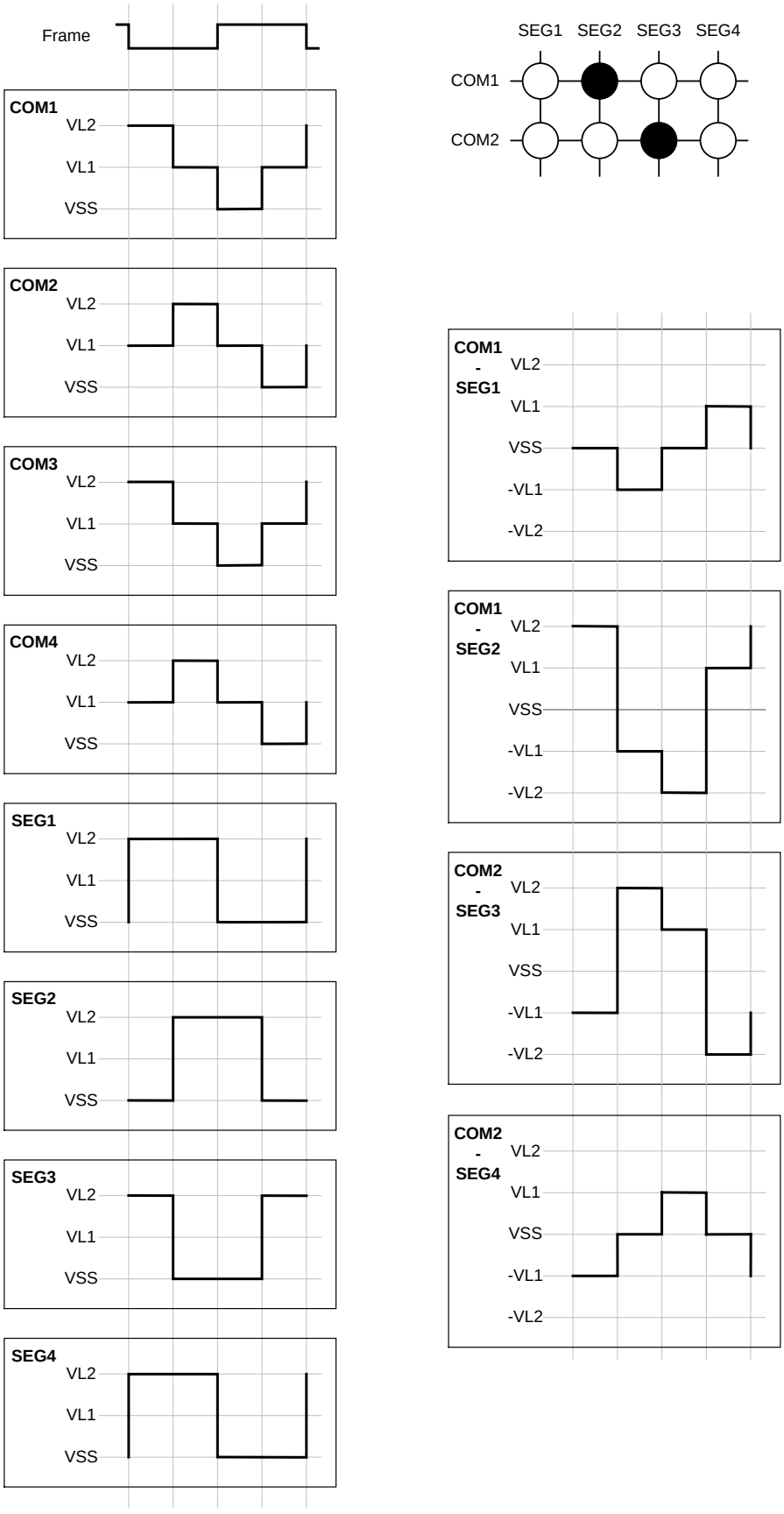



**Figure 2-2 : LCD Driver Waveforms – Mux2 & Bias ½ mode**

### 2.1.1.3. MUX2 & BIAS ⅓ MODE

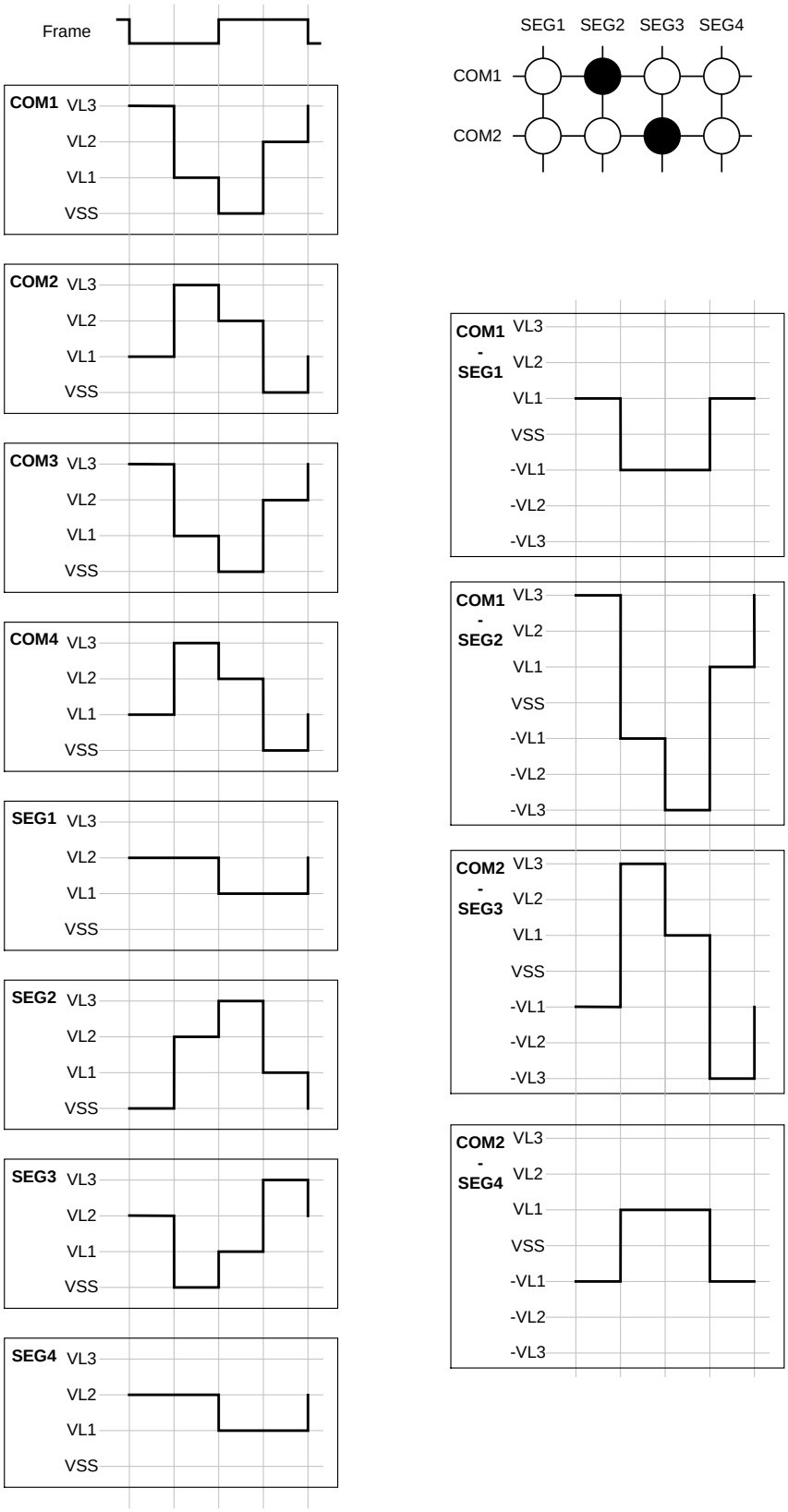



**Figure 2-3 : LCD Driver Waveforms – Mux2 & Bias ⅓ mode**

### 2.1.1.4. MUX3 & BIAS ½ MODE

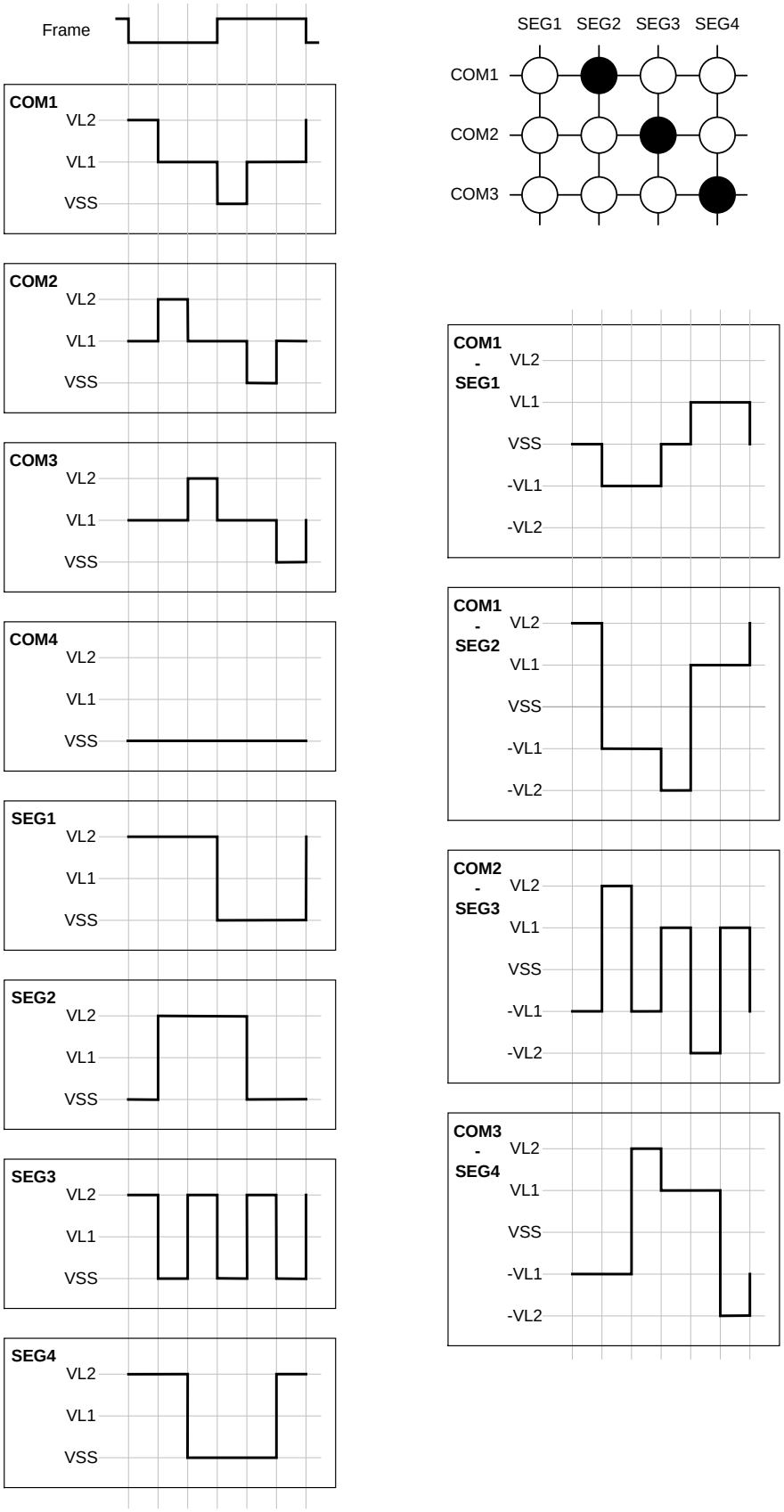



**Figure 2-4 : LCD Driver Waveforms – Mux3 & Bias ½ mode**

### 2.1.1.5. MUX3 & BIAS ⅓ MODE

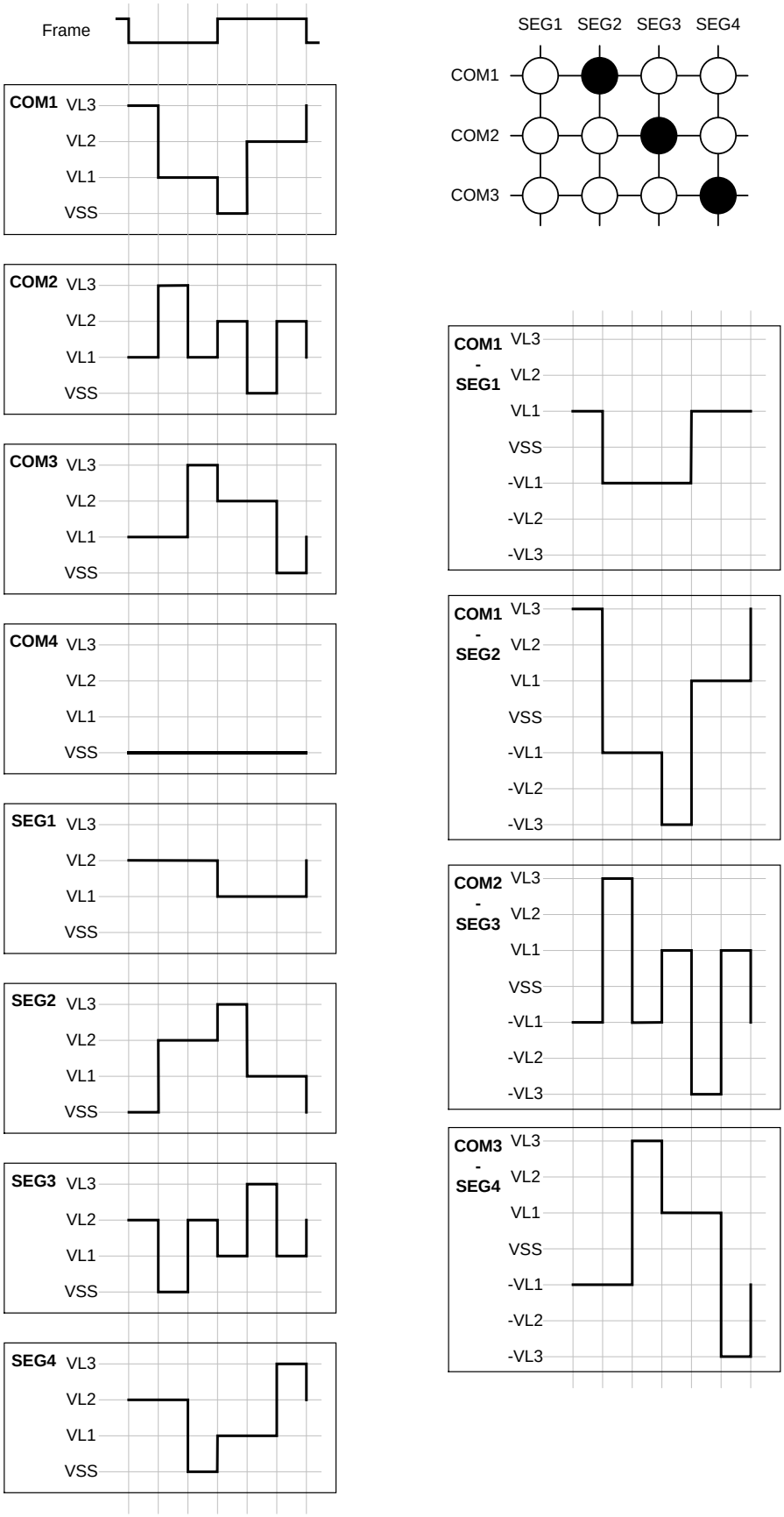



**Figure 2-5 : LCD Driver Waveforms – Mux3 & Bias ⅓ mode**

### 2.1.1.6. MUX4 & BIAS ½ MODE

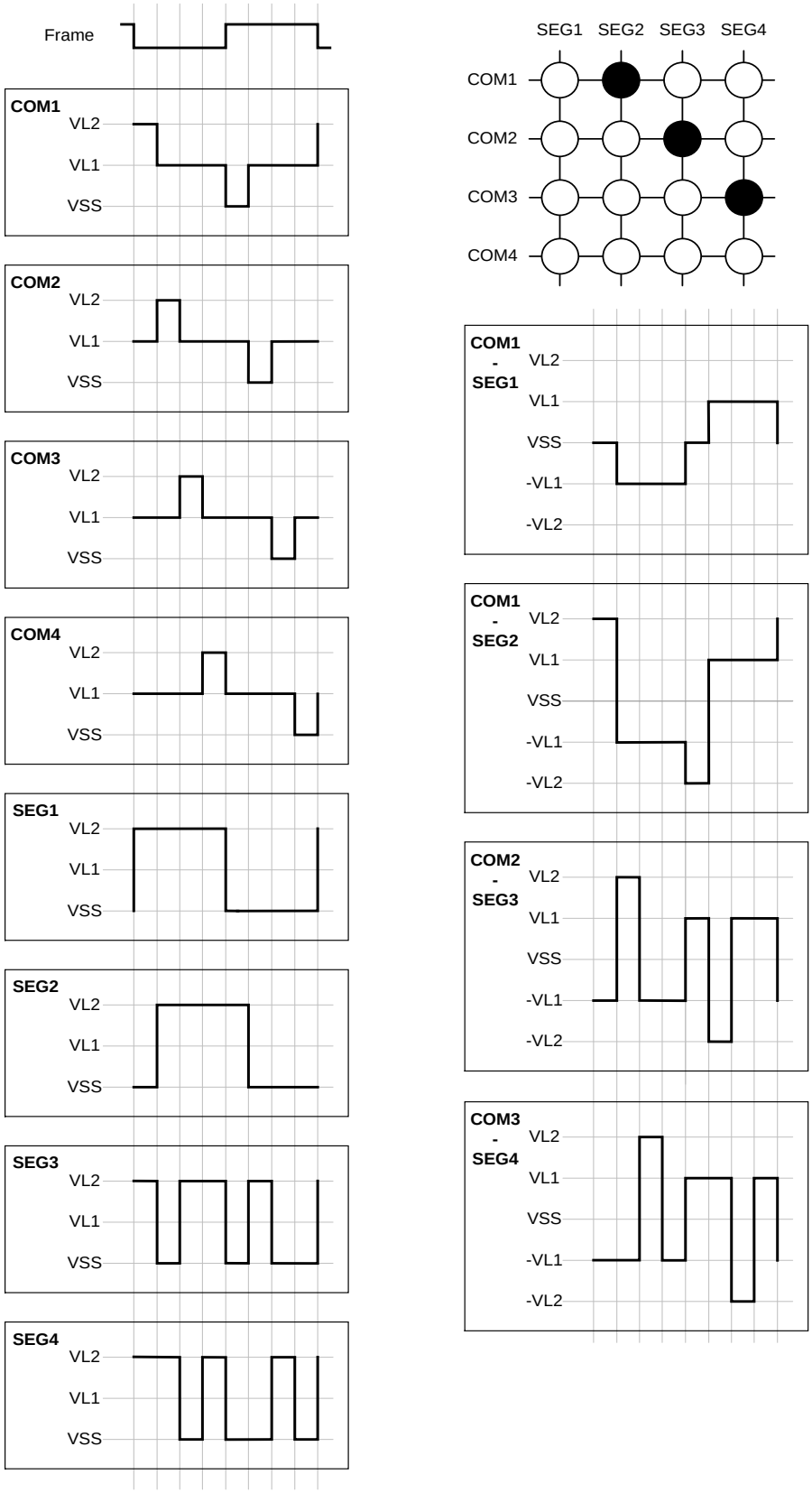



**Figure 2-6 : LCD Driver Waveforms – Mux4 & Bias ½ mode**

### 2.1.1.7. MUX4 & BIAS ⅓ MODE

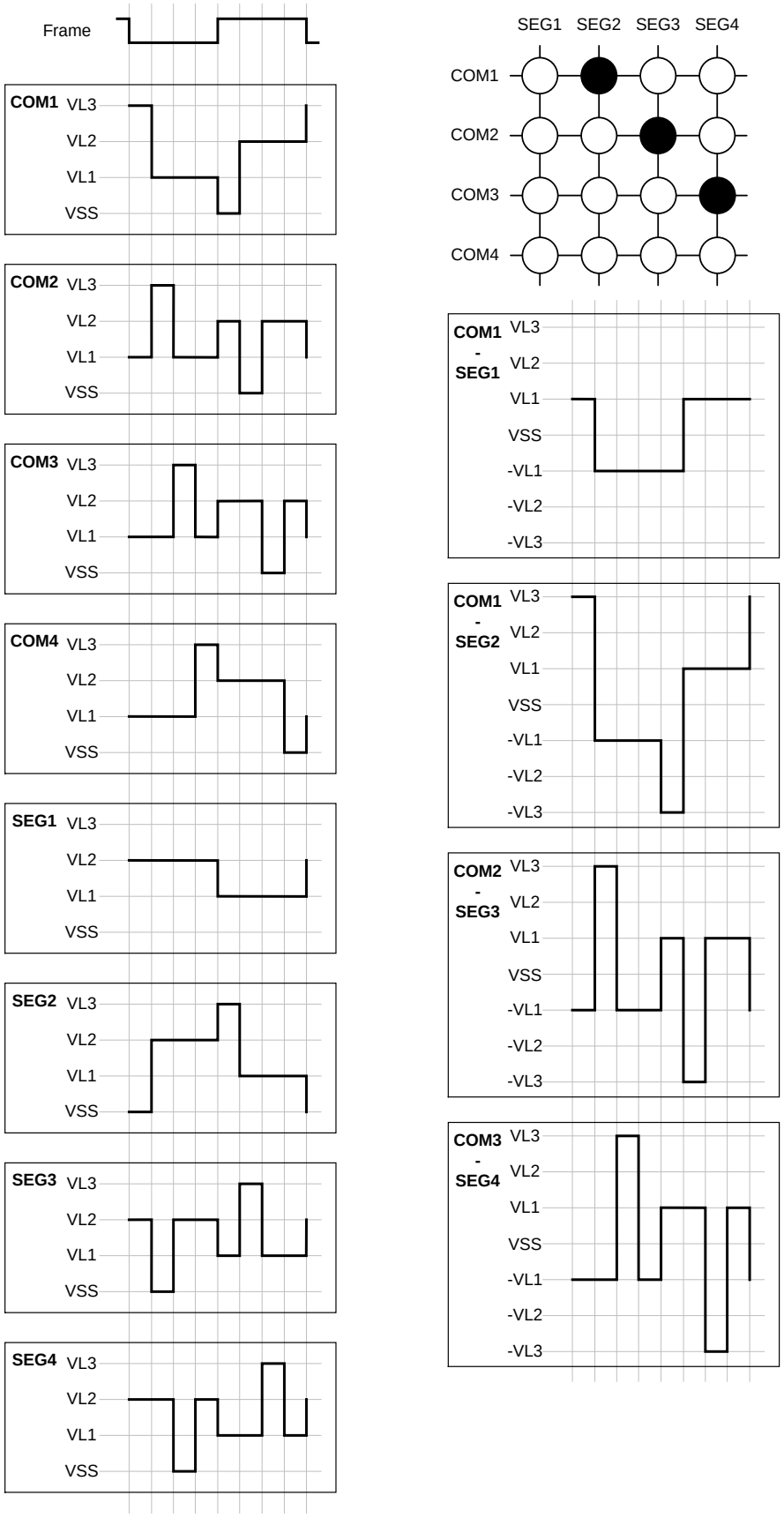



**Figure 2-7 : LCD Driver Waveforms – Mux4 & Bias ⅓ mode**

### 2.1.2. $V_{REF}$ REFERENCE

The internal voltage $V_{REF}$ is used as the reference for the generation of the LCD supply voltages. It is programmable by 25 mV steps. The "Vref_Level" bits set its value: $V_{REF}$ (V) = 0.8 + 0.025 x Vref_Level = 0.8 V … 2.375 V, with Vref_Level = [0, 63].

However, the supply voltage of the circuit can limit the maximum value of $V_{REF}$ and therefore the possible Vref_Level values by the following condition: VDD ≥ 1.05 x $V_{REF}$. For example, if VDD = 1.5 V then the maximum value is $V_{REF}$ = 1.425 V and thus the Vref_Level values are limited to the range [0, 25].

In Mux2, Mux3 and Mux4 there are two functional modes: Normal and Low Power mode. Depending on the selected mode, $V_{REF}$ is either connected to VL1 or VL2. The selected mode also determines the value of the external capacitors $C_{VL1}$ and $C_{VL2}$, where $C_{VL1}$ is connected to the pin VL1 and $C_{VL2}$ is connected to the pin VL2 (see section 2.9.5 for further information about the capacitors).

| Mode | Connection | $C_{VL1}$ | $C_{VL2}$ |
|---|---|---|---|
| Normal | $V_{REF}$ = VL1 | 1 µF | 100 nF |
| Low Power | $V_{REF}$ = VL2 | 100 nF | 1 µF |

**Table 2-2 : $V_{REF}$ connection and capacitors value in Mux2, Mux3 & Mux4**

### 2.1.3. STATIC DRIVE

In static drive there are four different $V_{ON}$ voltages that can be chosen: $V_{REF}$ / 2, $V_{REF}$, 2 x $V_{REF}$ or 3 x $V_{REF}$. Voltage $V_{REF}$ / 2 is generated by dividing the voltage reference by 2, voltage $V_{REF}$ is equal to the reference, and voltages 2 x $V_{REF}$ and 3 x $V_{REF}$ are generated by multiplying the reference by 2 and 3 respectively. The choice determines the value of the external capacitors $C_{VL1}$ and $C_{VL2}$ (see section 2.9.5 for further information about the capacitors). If $V_{REF}$ is chosen, only a 1 µF capacitor is necessary.

| Static drive options | | $C_{VL1}$ | $C_{VL2}$ |
|---|---|---|---|
| $V_{ON}$ = | $V_{REF}$ / 2 | 100 nF | 1 µF |
| | $V_{REF}$ | 1 µF | - |
| | 2 x $V_{REF}$ | 1 µF | 100 nF |
| | 3 x $V_{REF}$ | 1 µF | 100 nF |

**Table 2-3 : $V_{ON}$ options and capacitors value in Static drive**

In terms of system power consumption, the $V_{ON}$ = $V_{REF}$ / 2 option is the lowest one. The power consumption of the four options can be ordered in the following way: $I_{VREF/2}$ < $I_{VREF}$ < $I_{2xVREF}$ < $I_{3xVREF}$. However, the supply voltage of the circuit can limit the $V_{ON}$ choice (see section 2.1.2).

As can be seen in the Table 2-4, the range Vref_Level = [0, 63] is not fully valid for the four different $V_{ON}$ choices (due to technology boundaries): VL1, VL2 and VL3 voltages may range from 0.8 V to 3.3 V. In both static and multiplex drives, if a non-valid Vref_Level value is set the internal logic automatically uses the closest valid value. For example in static drive and $V_{ON}$ = $V_{REF}$ / 2, Vref_Level = 10 is non-valid and the circuit would assign the value 32.

| Static Drive - Condition: VDD ≥ 1.05 x $V_{REF}$ | | | | |
|---|---|---|---|---|
| | $V_{ON}$ (V) | | | |
| Vref_Level | $V_{REF}$ / 2 | $V_{REF}$ | 2 x $V_{REF}$ | 3 x $V_{REF}$ |
| 0 | 0.800 | 0.800 | 1.600 | 2.400 |
| 1 | 0.800 | 0.825 | 1.650 | 2.475 |
| 2 | 0.800 | 0.850 | 1.700 | 2.550 |
| 3 | 0.800 | 0.875 | 1.750 | 2.625 |
| 4 | 0.800 | 0.900 | 1.800 | 2.700 |
| 5 | 0.800 | 0.925 | 1.850 | 2.775 |
| 6 | 0.800 | 0.950 | 1.900 | 2.850 |
| 7 | 0.800 | 0.975 | 1.950 | 2.925 |
| 8 | 0.800 | 1.000 | 2.000 | 3.000 |
| 9 | 0.800 | 1.025 | 2.050 | 3.075 |
| 10 | 0.800 | 1.050 | 2.100 | 3.150 |
| 11 | 0.800 | 1.075 | 2.150 | 3.225 |

| Static Drive - Condition: VDD ≥ 1.05 x $V_{REF}$ | | | | |
|---|---|---|---|---|
| | $V_{ON}$ (V) | | | |
| Vref_Level | $V_{REF}$ / 2 | $V_{REF}$ | 2 x $V_{REF}$ | 3 x $V_{REF}$ |
| 12 | 0.800 | 1.100 | 2.200 | 3.300 |
| 13 | 0.800 | 1.125 | 2.250 | 3.300 |
| 14 | 0.800 | 1.150 | 2.300 | 3.300 |
| 15 | 0.800 | 1.175 | 2.350 | 3.300 |
| 16 | 0.800 | 1.200 | 2.400 | 3.300 |
| 17 | 0.800 | 1.225 | 2.450 | 3.300 |
| 18 | 0.800 | 1.250 | 2.500 | 3.300 |
| 19 | 0.800 | 1.275 | 2.550 | 3.300 |
| 20 | 0.800 | 1.300 | 2.600 | 3.300 |
| 21 | 0.800 | 1.325 | 2.650 | 3.300 |
| 22 | 0.800 | 1.350 | 2.700 | 3.300 |
| 23 | 0.800 | 1.375 | 2.750 | 3.300 |
| 24 | 0.800 | 1.400 | 2.800 | 3.300 |
| 25 | 0.800 | 1.425 | 2.850 | 3.300 |
| 26 | 0.800 | 1.450 | 2.900 | 3.300 |
| 27 | 0.800 | 1.475 | 2.950 | 3.300 |
| 28 | 0.800 | 1.500 | 3.000 | 3.300 |
| 29 | 0.800 | 1.525 | 3.050 | 3.300 |
| 30 | 0.800 | 1.550 | 3.100 | 3.300 |
| 31 | 0.800 | 1.575 | 3.150 | 3.300 |
| 32 | 0.800 | 1.600 | 3.200 | 3.300 |
| 33 | 0.812 | 1.625 | 3.250 | 3.300 |
| 34 | 0.825 | 1.650 | 3.300 | 3.300 |
| 35 | 0.837 | 1.675 | 3.300 | 3.300 |
| 36 | 0.850 | 1.700 | 3.300 | 3.300 |
| 37 | 0.862 | 1.725 | 3.300 | 3.300 |
| 38 | 0.875 | 1.750 | 3.300 | 3.300 |
| 39 | 0.887 | 1.775 | 3.300 | 3.300 |
| 40 | 0.900 | 1.800 | 3.300 | 3.300 |
| 41 | 0.912 | 1.825 | 3.300 | 3.300 |
| 42 | 0.925 | 1.850 | 3.300 | 3.300 |
| 43 | 0.937 | 1.875 | 3.300 | 3.300 |
| 44 | 0.950 | 1.900 | 3.300 | 3.300 |
| 45 | 0.962 | 1.925 | 3.300 | 3.300 |
| 46 | 0.975 | 1.950 | 3.300 | 3.300 |
| 47 | 0.987 | 1.975 | 3.300 | 3.300 |
| 48 | 1.000 | 2.000 | 3.300 | 3.300 |
| 49 | 1.013 | 2.025 | 3.300 | 3.300 |
| 50 | 1.025 | 2.050 | 3.300 | 3.300 |
| 51 | 1.038 | 2.075 | 3.300 | 3.300 |
| 52 | 1.050 | 2.100 | 3.300 | 3.300 |
| 53 | 1.063 | 2.125 | 3.300 | 3.300 |
| 54 | 1.075 | 2.150 | 3.300 | 3.300 |
| 55 | 1.088 | 2.175 | 3.300 | 3.300 |
| 56 | 1.100 | 2.200 | 3.300 | 3.300 |
| 57 | 1.113 | 2.225 | 3.300 | 3.300 |
| 58 | 1.125 | 2.250 | 3.300 | 3.300 |
| 59 | 1.138 | 2.275 | 3.300 | 3.300 |
| 60 | 1.150 | 2.300 | 3.300 | 3.300 |
| 61 | 1.163 | 2.325 | 3.300 | 3.300 |
| 62 | 1.175 | 2.350 | 3.300 | 3.300 |
| 63 | 1.188 | 2.375 | 3.300 | 3.300 |

**Table 2-4 : $V_{ON}$ in Static Drive**

### 2.1.4. MULTIPLEX DRIVE: NORMAL MODE

In this mode $V_{REF}$ = VL1, Vref_Level = [0, 34] for bias ½ and Vref_Level = [0, 12] for bias ⅓. Table 2-5 and Table 2-6 show all the $V_{ON}$ and $V_{OFF}$ values: as can be seen, the supply voltage of the circuit can limit the possible $V_{ON}$ and $V_{OFF}$ values. In Normal mode: $C_{VL1}$ = 1 µF and $C_{VL2}$ = 100 nF.

| Bias ½ - Condition: VDD ≥ 1.05 x $V_{REF}$ | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | Mux2 | | Mux3 | | Mux4 | |
| Vref_Level | $V_{REF}$ = VL1 (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) |
| 0 | 0.800 | 1.265 | 0.566 | 1.131 | 0.653 | 1.058 | 0.693 |
| 1 | 0.825 | 1.304 | 0.583 | 1.167 | 0.674 | 1.091 | 0.714 |
| 2 | 0.850 | 1.344 | 0.601 | 1.202 | 0.694 | 1.124 | 0.736 |
| 3 | 0.875 | 1.383 | 0.619 | 1.237 | 0.714 | 1.158 | 0.758 |
| 4 | 0.900 | 1.423 | 0.636 | 1.273 | 0.735 | 1.191 | 0.779 |
| 5 | 0.925 | 1.463 | 0.654 | 1.308 | 0.755 | 1.224 | 0.801 |
| 6 | 0.950 | 1.502 | 0.672 | 1.344 | 0.776 | 1.257 | 0.823 |
| 7 | 0.975 | 1.542 | 0.689 | 1.379 | 0.796 | 1.290 | 0.844 |
| 8 | 1.000 | 1.581 | 0.707 | 1.414 | 0.816 | 1.323 | 0.866 |
| 9 | 1.025 | 1.621 | 0.725 | 1.450 | 0.837 | 1.356 | 0.888 |
| 10 | 1.050 | 1.660 | 0.742 | 1.485 | 0.857 | 1.389 | 0.909 |
| 11 | 1.075 | 1.700 | 0.760 | 1.520 | 0.878 | 1.422 | 0.931 |
| 12 | 1.100 | 1.739 | 0.778 | 1.556 | 0.898 | 1.455 | 0.953 |
| 13 | 1.125 | 1.779 | 0.795 | 1.591 | 0.919 | 1.488 | 0.974 |
| 14 | 1.150 | 1.818 | 0.813 | 1.626 | 0.939 | 1.521 | 0.996 |
| 15 | 1.175 | 1.858 | 0.831 | 1.662 | 0.959 | 1.554 | 1.018 |
| 16 | 1.200 | 1.897 | 0.849 | 1.697 | 0.980 | 1.587 | 1.039 |
| 17 | 1.225 | 1.937 | 0.866 | 1.732 | 1.000 | 1.621 | 1.061 |
| 18 | 1.250 | 1.976 | 0.884 | 1.769 | 1.021 | 1.654 | 1.083 |
| 19 | 1.275 | 2.016 | 0.902 | 1.803 | 1.041 | 1.687 | 1.104 |
| 20 | 1.300 | 2.055 | 0.919 | 1.838 | 1.061 | 1.720 | 1.126 |
| 21 | 1.325 | 2.095 | 0.937 | 1.874 | 1.082 | 1.753 | 1.147 |
| 22 | 1.350 | 2.135 | 0.955 | 1.909 | 1.102 | 1.786 | 1.169 |
| 23 | 1.375 | 2.174 | 0.972 | 1.945 | 1.123 | 1.819 | 1.191 |
| 24 | 1.400 | 2.214 | 0.990 | 1.980 | 1.143 | 1.852 | 1.212 |
| 25 | 1.425 | 2.253 | 1.008 | 2.015 | 1.164 | 1.885 | 1.234 |
| 26 | 1.450 | 2.293 | 1.025 | 2.051 | 1.184 | 1.918 | 1.256 |
| 27 | 1.475 | 2.332 | 1.043 | 2.086 | 1.204 | 1.951 | 1.277 |
| 28 | 1.500 | 2.372 | 1.061 | 2.121 | 1.225 | 1.984 | 1.299 |
| 29 | 1.525 | 2.411 | 1.078 | 2.157 | 1.245 | 2.017 | 1.321 |
| 30 | 1.550 | 2.451 | 1.096 | 2.192 | 1.266 | 2.050 | 1.342 |
| 31 | 1.575 | 2.490 | 1.114 | 2.227 | 1.286 | 2.084 | 1.364 |
| 32 | 1.600 | 2.530 | 1.131 | 2.263 | 1.306 | 2.117 | 1.386 |
| 33 | 1.625 | 2.569 | 1.149 | 2.298 | 1.327 | 2.150 | 1.407 |
| 34 | 1.650 | 2.609 | 1.167 | 2.333 | 1.347 | 2.183 | 1.429 |
| 35 ... 63 | 1.650 | 2.609 | 1.167 | 2.333 | 1.347 | 2.183 | 1.429 |

**Table 2-5 : $V_{ON}$ and $V_{OFF}$ in Bias ½ for Mux 2, 3 & 4 (Normal mode)**

| Bias ⅓ - Condition: VDD ≥ 1.05 x $V_{REF}$ | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | Mux2 | | Mux3 | | Mux4 | |
| Vref_Level | $V_{REF}$ = VL1 (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) |
| 0 | 0.800 | 1.789 | 0.800 | 1.532 | 0.800 | 1.386 | 0.800 |
| 1 | 0.825 | 1.845 | 0.825 | 1.580 | 0.825 | 1.429 | 0.825 |
| 2 | 0.850 | 1.901 | 0.850 | 1.628 | 0.850 | 1.472 | 0.850 |
| 3 | 0.875 | 1.957 | 0.875 | 1.675 | 0.875 | 1.516 | 0.875 |
| 4 | 0.900 | 2.012 | 0.900 | 1.723 | 0.900 | 1.559 | 0.900 |
| 5 | 0.925 | 2.068 | 0.925 | 1.771 | 0.925 | 1.602 | 0.925 |
| 6 | 0.950 | 2.124 | 0.950 | 1.819 | 0.950 | 1.645 | 0.950 |
| 7 | 0.975 | 2.180 | 0.975 | 1.867 | 0.975 | 1.689 | 0.975 |
| 8 | 1.000 | 2.236 | 1.000 | 1.915 | 1.000 | 1.732 | 1.000 |
| 9 | 1.025 | 2.292 | 1.025 | 1.963 | 1.025 | 1.775 | 1.025 |
| 10 | 1.050 | 2.348 | 1.050 | 2.011 | 1.050 | 1.819 | 1.050 |
| 11 | 1.075 | 2.404 | 1.075 | 2.058 | 1.075 | 1.862 | 1.075 |
| 12 | 1.100 | 2.460 | 1.100 | 2.106 | 1.100 | 1.905 | 1.100 |
| 13 … 63 | 1.100 | 2.460 | 1.100 | 2.106 | 1.100 | 1.905 | 1.100 |

**Table 2-6 : $V_{ON}$ and $V_{OFF}$ in Bias ⅓ for Mux 2, 3 & 4 (Normal mode)**

## 2.1.5. MULTIPLEX DRIVE: LOW POWER MODE

The Low Power mode uses a novel technique that enables to further reduce the power consumption of the driver and the display. When both Normal mode and Low Power mode are available, the latter is recommended. However, the Low Power mode is only available when $V_{REF}$ ≥ 1.6 V and therefore when VDD ≥ 1.68 V.

In this mode, $V_{REF}$ = VL2, Vref_Level = [32, 63] for bias ½ and Vref_Level = [32, 56] for bias ⅓. Table 2-7 and Table 2-8 show all the $V_{ON}$ and $V_{OFF}$ values, and as in Normal mode, the supply voltage of the circuit can limit the possible $V_{ON}$ and $V_{OFF}$ values. In Low Power mode: $C_{VL1}$ = 100 nF and $C_{VL2}$ = 1 µF.

| Bias ½- Condition: VDD ≥ 1.05 x $V_{REF}$ | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | Mux2 | | Mux3 | | Mux4 | |
| Vref_Level | $V_{REF}$ = VL2 (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) |
| 0 … 31 | 1.600 | 1.265 | 0.566 | 1.131 | 0.653 | 1.058 | 0.693 |
| 32 | 1.600 | 1.265 | 0.566 | 1.131 | 0.653 | 1.058 | 0.693 |
| 33 | 1.625 | 1.285 | 0.575 | 1.149 | 0.663 | 1.075 | 0.704 |
| 34 | 1.650 | 1.304 | 0.583 | 1.167 | 0.674 | 1.091 | 0.714 |
| 35 | 1.675 | 1.324 | 0.592 | 1.184 | 0.684 | 1.108 | 0.725 |
| 36 | 1.700 | 1.344 | 0.601 | 1.202 | 0.694 | 1.124 | 0.736 |
| 37 | 1.725 | 1.364 | 0.610 | 1.220 | 0.704 | 1.141 | 0.747 |
| 38 | 1.750 | 1.383 | 0.619 | 1.237 | 0.714 | 1.158 | 0.758 |
| 39 | 1.775 | 1.403 | 0.628 | 1.255 | 0.725 | 1.174 | 0.769 |
| 40 | 1.800 | 1.423 | 0.636 | 1.273 | 0.735 | 1.191 | 0.779 |
| 41 | 1.825 | 1.443 | 0.645 | 1.290 | 0.745 | 1.207 | 0.790 |
| 42 | 1.850 | 1.463 | 0.654 | 1.308 | 0.755 | 1.224 | 0.801 |
| 43 | 1.875 | 1.482 | 0.663 | 1.326 | 0.765 | 1.240 | 0.812 |
| 44 | 1.900 | 1.502 | 0.672 | 1.344 | 0.776 | 1.257 | 0.823 |
| 45 | 1.925 | 1.522 | 0.681 | 1.361 | 0.786 | 1.273 | 0.834 |
| 46 | 1.950 | 1.542 | 0.689 | 1.379 | 0.796 | 1.290 | 0.844 |
| 47 | 1.975 | 1.561 | 0.698 | 1.397 | 0.806 | 1.306 | 0.855 |
| 48 | 2.000 | 1.581 | 0.707 | 1.414 | 0.816 | 1.323 | 0.866 |
| 49 | 2.025 | 1.601 | 0.716 | 1.432 | 0.827 | 1.339 | 0.877 |
| 50 | 2.050 | 1.621 | 0.725 | 1.450 | 0.837 | 1.356 | 0.888 |
| 51 | 2.075 | 1.640 | 0.734 | 1.467 | 0.847 | 1.372 | 0.899 |
| 52 | 2.100 | 1.660 | 0.742 | 1.485 | 0.857 | 1.389 | 0.909 |
| 53 | 2.125 | 1.680 | 0.751 | 1.503 | 0.868 | 1.406 | 0.920 |
| 54 | 2.150 | 1.700 | 0.760 | 1.520 | 0.878 | 1.422 | 0.931 |
| 55 | 2.175 | 1.719 | 0.769 | 1.538 | 0.888 | 1.439 | 0.942 |

| Bias ½- Condition: VDD ≥ 1.05 x $V_{REF}$ | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | Mux2 | | Mux3 | | Mux4 | |
| Vref_Level | $V_{REF}$ = VL2 (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) |
| 56 | 2.200 | 1.739 | 0.778 | 1.556 | 0.898 | 1.455 | 0.953 |
| 57 | 2.225 | 1.759 | 0.787 | 1.573 | 0.908 | 1.472 | 0.963 |
| 58 | 2.250 | 1.779 | 0.795 | 1.591 | 0.919 | 1.488 | 0.974 |
| 59 | 2.275 | 1.799 | 0.804 | 1.609 | 0.929 | 1.505 | 0.985 |
| 60 | 2.300 | 1.818 | 0.813 | 1.626 | 0.939 | 1.521 | 0.996 |
| 61 | 2.325 | 1.838 | 0.822 | 1.644 | 0.949 | 1.538 | 1.007 |
| 62 | 2.350 | 1.858 | 0.831 | 1.662 | 0.959 | 1.554 | 1.018 |
| 63 | 2.375 | 1.878 | 0.840 | 1.679 | 0.970 | 1.571 | 1.028 |

**Table 2-7 : $V_{ON}$ and $V_{OFF}$ in Bias ½ for Mux 2, 3 & 4 (Low Power mode)**

| Bias ⅓ - Condition: VDD ≥ 1.05 x $V_{REF}$ | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | Mux2 | | Mux3 | | Mux4 | |
| Vref_Level | $V_{REF}$ = VL2 (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) | $V_{ON}$ (V) | $V_{OFF}$ (V) |
| 0 … 31 | 1.600 | 1.789 | 0.800 | 1.532 | 0.800 | 1.386 | 0.800 |
| 32 | 1.600 | 1.789 | 0.800 | 1.532 | 0.800 | 1.386 | 0.800 |
| 33 | 1.625 | 1.817 | 0.813 | 1.556 | 0.813 | 1.407 | 0.813 |
| 34 | 1.650 | 1.845 | 0.825 | 1.580 | 0.825 | 1.429 | 0.825 |
| 35 | 1.675 | 1.873 | 0.838 | 1.604 | 0.838 | 1.451 | 0.838 |
| 36 | 1.700 | 1.901 | 0.850 | 1.628 | 0.850 | 1.472 | 0.850 |
| 37 | 1.725 | 1.929 | 0.863 | 1.652 | 0.863 | 1.494 | 0.863 |
| 38 | 1.750 | 1.957 | 0.875 | 1.675 | 0.875 | 1.516 | 0.875 |
| 39 | 1.775 | 1.985 | 0.888 | 1.699 | 0.888 | 1.537 | 0.888 |
| 40 | 1.800 | 2.012 | 0.900 | 1.723 | 0.900 | 1.559 | 0.900 |
| 41 | 1.825 | 2.040 | 0.913 | 1.747 | 0.913 | 1.580 | 0.913 |
| 42 | 1.850 | 2.068 | 0.925 | 1.771 | 0.925 | 1.602 | 0.925 |
| 43 | 1.875 | 2.096 | 0.938 | 1.795 | 0.938 | 1.624 | 0.938 |
| 44 | 1.900 | 2.124 | 0.950 | 1.819 | 0.950 | 1.645 | 0.950 |
| 45 | 1.925 | 2.152 | 0.962 | 1.843 | 0.962 | 1.667 | 0.962 |
| 46 | 1.950 | 2.180 | 0.975 | 1.867 | 0.975 | 1.689 | 0.975 |
| 47 | 1.975 | 2.208 | 0.987 | 1.891 | 0.987 | 1.710 | 0.987 |
| 48 | 2.000 | 2.236 | 1.000 | 1.915 | 1.000 | 1.732 | 1.000 |
| 49 | 2.025 | 2.264 | 1.013 | 1.939 | 1.013 | 1.754 | 1.013 |
| 50 | 2.050 | 2.292 | 1.025 | 1.963 | 1.025 | 1.775 | 1.025 |
| 51 | 2.075 | 2.320 | 1.038 | 1.987 | 1.038 | 1.797 | 1.038 |
| 52 | 2.100 | 2.348 | 1.050 | 2.011 | 1.050 | 1.819 | 1.050 |
| 53 | 2.125 | 2.376 | 1.063 | 2.035 | 1.063 | 1.840 | 1.063 |
| 54 | 2.150 | 2.404 | 1.075 | 2.058 | 1.075 | 1.862 | 1.075 |
| 55 | 2.175 | 2.432 | 1.088 | 2.082 | 1.088 | 1.884 | 1.088 |
| 56 | 2.200 | 2.460 | 1.100 | 2.106 | 1.100 | 1.905 | 1.100 |
| 57 … 63 | 2.200 | 2.460 | 1.100 | 2.106 | 1.100 | 1.905 | 1.100 |

**Table 2-8 : $V_{ON}$ and $V_{OFF}$ in Bias ⅓ for Mux 2, 3 & 4 (Low Power mode)**

## 2.2. PROGRAMMABLE GROUPS OF LCD SEGMENTS

The LCD segments are defined in a logical view, independently of their physical arrangement. This view consists of a given number of groups, of up to eight segments each; in the case of the EM6115, you are given 32 groups of 8 segments and you can address each segment independently of the others, without taking care of its physical or multiplex connection. The aim of this idea is to reduce the overall number of data transfers in the system by an efficient grouping of the segments.

The translation from the logical to the physical segments is done through a so-named mapping dictionary, where you must define for each physical segment, to which logical group and to which individual bit of this group it belongs. By this way, you can group all the segments of a digit in the same logical group and define a common group for the symbols spread around the LCD. The programming of the mapping dictionary can be done either by a user command or directly from the embedded EEPROM at startup.

### 2.2.1. LOGICAL SEGMENTS AND GROUPS

The LCD segments are activated by writing values in the group registers (named GroupX in chapter 2.7.3) or in the group individual blink registers (named Blk_GrX in chapter 2.7.3). Each group register is identified by a suffix number from 0 to 31, and each bit in a group is identified by a prefix letter: bit0 (LSBit) = A, bit 1 = B, bit 2 = C, bit 3 = D … bit 7 (MSBit) = H.

For example, the bit 0 of the group 0 is named A0, the bit 7 of the group 3 H3, the bit 6 of the group 14 G14. These bit names are used for the segment activation and for the mapping dictionary definition.

The internal decoding mechanism is designed towards ultra-low power consumption: you can only write to the group or individual blink registers, but you cannot readback these registers, nor the current active physical segments.

### 2.2.2. DICTIONARY

In the mapping dictionary each physical LCD segment is defined by its group number and its group bit. Five (5) bits are necessary to code the group number (Ngrp[4:0]) and three (3) bits for the group bit (Nbit[2:0]).

| Group bit position | Group bit prefix | Nbit[2:0] |
|---|---|---|
| 0 (LSBit) | A | 000 |
| 1 | B | 001 |
| 2 | C | 010 |
| 3 | D | 011 |
| 4 | E | 100 |
| 5 | F | 101 |
| 6 | G | 110 |
| 7 (MSBit) | H | 111 |

**Table 2-9 : Correspondence of Nbit[2:0]**

The mapping dictionary can be written by the MCU with the command “WRITE_DIC” (see chapter 2.4). This command is incremental, i.e. it starts defining the group number and the group bit for the combination SEG[1] & COM[1] and continues with the following combinations. The communication transfer can be seen in the Table 2-10.

| Byte | Word | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | WRITE_DIC | $20 | | | | | | | |
| 1 | SEG[1] & COM[1] | Ngrp_011[4:0] | | | | | Nbit_011[2:0] | | |
| 2 | SEG[1] & COM[2] | Ngrp_012[4:0] | | | | | Nbit_012[2:0] | | |
| 3 | SEG[1] & COM[3] | Ngrp_013[4:0] | | | | | Nbit_013[2:0] | | |
| 4 | SEG[1] & COM[4] | Ngrp_014[4:0] | | | | | Nbit_014[2:0] | | |
| 5 | SEG[2] & COM[1] | Ngrp_021[4:0] | | | | | Nbit_021[2:0] | | |
| 6 | SEG[2] & COM[2] | Ngrp_022[4:0] | | | | | Nbit_022[2:0] | | |
| … | … | … | | | | | … | | |
| 199 | SEG[50] & COM[3] | Ngrp_503[4:0] | | | | | Nbit_503[2:0] | | |
| 200 | SEG[50] & COM[4] | Ngrp_504[4:0] | | | | | Nbit_504[2:0] | | |

**Table 2-10 : Communication transfer for “WRITE_DIC” command**

Multiple physical LCD segments can be defined with the same group number and group bit. In that case, the LCD segments are controlled by the same bit in the functional registers and, therefore, they are linked together.

It is not necessary to write the mapping dictionary for all the possible combinations if they are not used. It is sufficient to send the group number and the group bit from the SEG[1] & COM[1] combination to the last used SEG & COM combination. By default, the unused combinations are defined as logical segment A0. In that case, the bit A of the Group0 should not be used to define any used and valid combination. However, all the combinations from SEG[1] & COM[1] to the last used SEG & COM must be defined even if they are not used. For example, if MUX2 is used, the combinations using COM[3] and COM[4] must be defined as well. One option would be to define all of them as logical segment A0.

### 2.2.3. EXAMPLE DICTIONARY

The Figure 2-8 shows a typical physical segment design (gray zone) and its connection to the LCD controller in MUX2 mode. The segment-LCD is represented by the combination of SEG and COM lines that drives it. In this example, the segments of the first 7-segment digit are ordered in the same group independently of the connection to the driver. However and as can be seen in the two other digits of this example, this grouping is not the only possibility.

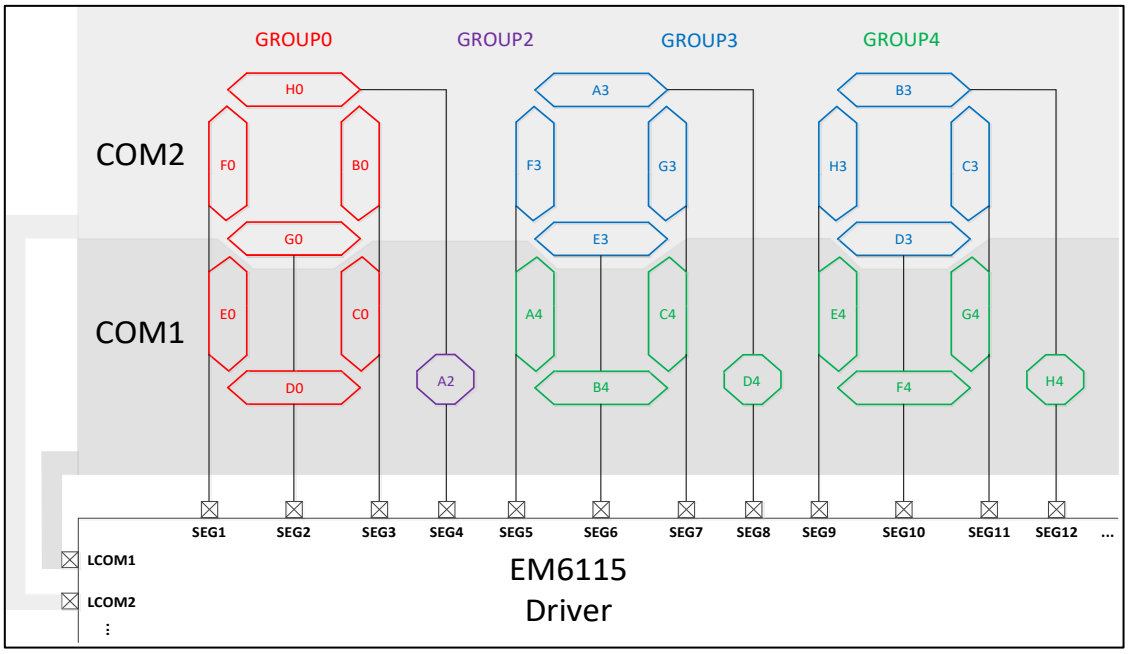



**Figure 2-8 : Groups definition example**

The mapping dictionary is shown in Table 2-11 and defines how the LCD segments are ordered into groups. The Table 2-12 shows the beginning of the communication transfer to setup the dictionary of the example; the unused physical segments are included in this transfer (segments addressed with COM[3] and COM[4]), but the length of the transfer is strictly limited to the connected segments (SEG[12])

| SEG | COM | Group | Bit | Bit name |
|---|---|---|---|---|
| SEG1 | COM1 | 0 | 4 | E0 |
| SEG1 | COM2 | 0 | 5 | F0 |
| SEG2 | COM1 | 0 | 3 | D0 |
| SEG2 | COM2 | 0 | 6 | G0 |
| SEG3 | COM1 | 0 | 2 | C0 |
| SEG3 | COM2 | 0 | 1 | B0 |
| SEG4 | COM1 | 2 | 0 | A2 |
| SEG4 | COM2 | 0 | 7 | H0 |
| SEG5 | COM1 | 4 | 0 | A4 |
| SEG5 | COM2 | 3 | 5 | F3 |
| SEG6 | COM1 | 4 | 1 | B4 |
| SEG6 | COM2 | 3 | 4 | E3 |
| SEG7 | COM1 | 4 | 2 | C4 |
| SEG7 | COM2 | 3 | 6 | G3 |
| SEG8 | COM1 | 4 | 3 | D4 |
| SEG8 | COM2 | 3 | 0 | A3 |
| SEG9 | COM1 | 4 | 4 | E4 |
| SEG9 | COM2 | 3 | 7 | H3 |
| SEG10 | COM1 | 4 | 5 | F4 |
| SEG10 | COM2 | 3 | 3 | D3 |
| SEG11 | COM1 | 4 | 6 | G4 |
| SEG11 | COM2 | 3 | 2 | C3 |
| SEG12 | COM1 | 4 | 7 | H4 |
| SEG12 | COM2 | 3 | 1 | B3 |

**Table 2-11 : Dictionary example**

| Byte | Word | Content |
|---|---|---|
| 0 | WRITE_DIC | $20 |
| 1 | SEG[1] & COM[1] | $04 |
| 2 | SEG[1] & COM[2] | $05 |
| 3 | SEG[1] & COM[3] | $00 (non-used) |
| 4 | SEG[1] & COM[4] | $00 (non-used) |
| 5 | SEG[2] & COM[1] | $03 |
| 6 | SEG[2] & COM[2] | $06 |
| 7 | SEG[2] & COM[3] | $00 (non-used) |
| 8 | SEG[2] & COM[4] | $00 (non-used) |
| 9 | SEG[3] & COM[1] | $02 |
| 10 | SEG[3] & COM[2] | $01 |
| 11 | SEG[3] & COM[3] | $00 (non-used) |
| 12 | SEG[3] & COM[4] | $00 (non-used) |
| 13 | SEG[4] & COM[1] | $10 |
| 14 | SEG[4] & COM[2] | $07 |
| 15 | SEG[4] & COM[3] | $00 (non-used) |
| 16 | SEG[4] & COM[4] | $00 (non-used) |
| 17 | SEG[5] & COM[1] | $20 |
| … | … | … |
| 45 | SEG[12] & COM[1] | $27 |
| 46 | SEG[12] & COM[2] | $19 |

**Table 2-12 : Dictionary setup of the example (section 2.2)**

Referring to the example described above, the Figure 2-9 and the Table 2-13 show an active display and the corresponding communication data transfers. In the first transfer the address is $40 (Group0). The group value is equal to $CE that in this example means lighting the number 3 in the first 7-segment digit. Afterwards a new transfer is done starting at Group2 with a group value of $01. Notice that if the transfer continues, the next byte is the group value of address group incremented by one, in this case Group3, as specified in the section 2.7.

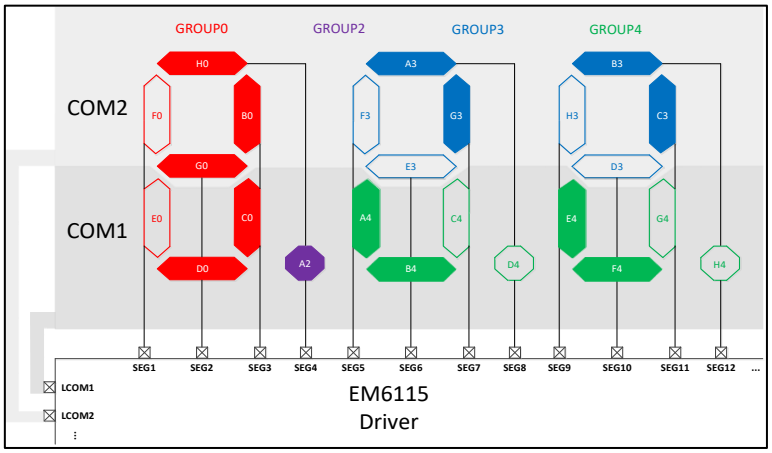



**Figure 2-9 : Example of active segments**

| Com Transfer | Content | Byte | Group |
|---|---|---|---|
| 1 | WRITE_REG address 0 | $40 | - |
| 1 | Value | $CE | 0 |
| 2 | WRITE_REG address 2 | $42 | - |
| 2 | Value | $01 | 2 |
| 2 | Value | $47 | 3 |
| 2 | Value | $33 | 4 |

**Table 2-13 : Example of group write transfer**

## 2.3. COMMUNICATION INTERFACE

The communication interface is slave only and allows a synchronous and serial communication between the host and the device. The interface is selected through the CIS pin. If CIS is low, the SPI interface is selected. If CIS is high, the I²C interface is used. A transfer begins with a command followed by data until the transfer is stopped (STOP condition with I²C interface or nSS driven high for SPI). The internal register address pointer is automatically incremented in case of multiple-byte access. The communication interface configuration must not be modified while the circuit is active: pin EN = VDD.

| Pins | CIS = VDD | | | CIS = VSS | | |
|---|---|---|---|---|---|---|
| | Name | Type | Description | Name | Type | Description |
| CIO0 | SCL | I/O | I²C clock | SCK | I | SPI Clock |
| CIO1 | SDA | I/O | I²C data | MOSI | I | SPI Data In |
| CIO2 | EN_IWPU | I | Enable I²C internal Weak pull-up resistors on CIO0 and CIO1 | MISO | O | SPI Data Out (if enabled), or Low Level Output |
| CI3 | EN_ISPU | I | Enable I²C internal Strong pull-up resistors on CIO0 and CIO1 | nSS | I | SPI Slave Select (Active low) |
| CI4 | A0 | I | I²C address bit 0 | - | - | Not-used |
| CI5 | A1 | I | I²C address bit 1 | CK_POL | I | SPI SCK Polarity |
| CI6 | A2 | I | I²C address bit 2 | CK_PHA | I | SPI SCK Phase |
| CI7 | A3 | I | I²C address bit 3 | MSB_FIRST | I | SPI MSB First selection |
| CI8 | ICRDY_POL | I | ICRDY polarity | ICRDY_POL | I | ICRDY polarity |

**Table 2-14 : Interface pins configuration**

### 2.3.1. I²C INTERFACE

The I²C is a 2-wire interface (serial clock and serial data). The serial clock (SCL) provides the timing for the interface. The serial data (SDA) is bidirectional and is used to transfer data, according to NXP UM10204 Specification (I2C-bus specification and user manual, Version 6.0, 4th of April 2014).

The I²C interface has the following restrictions:

- Only Standard-mode and Fast-mode are supported. Thus, the maximum clock frequency is 400 kHz.
- Only standard 7-bit addressing is supported. The default values of the 3 MSB are “001” while the 4 LSB are defined by A3…A0 input pins; the available address range is $10 to $1F.
- General Calls are ignored.
- Each I²C bidirectional pin can use a weak (40 kΩ) and/or a strong (20 kΩ) internal pull-up resistor. These resistors can be enabled by connecting respectively the EN_IWPU and/or EN_ISPU input pins to VDD, and this setting is independent of the global chip enable (pin EN). However, as these internal pull-up resistors have been designed to minimize power consumption, the capacitive bus loads are limited, even when both pull-up resistors are simultaneously enabled. For higher capacitive bus loads, external I²C pullup resistors must be added.
- Clock stretching is not supported.

Both data and clock lines remain high when the bus is not busy. A high to low transition of the data line, while the clock is high is defined as a START condition. A low to high transition of the data line while the clock is high is defined as a STOP condition. One data bit is transferred during each SCL pulse. The data on SDA line is sampled at the falling edge of the SCL line and must remain stable during the high period of SCL pulses, as any change at this time would be interpreted as a START or a STOP condition. Data is always transferred MSB first.

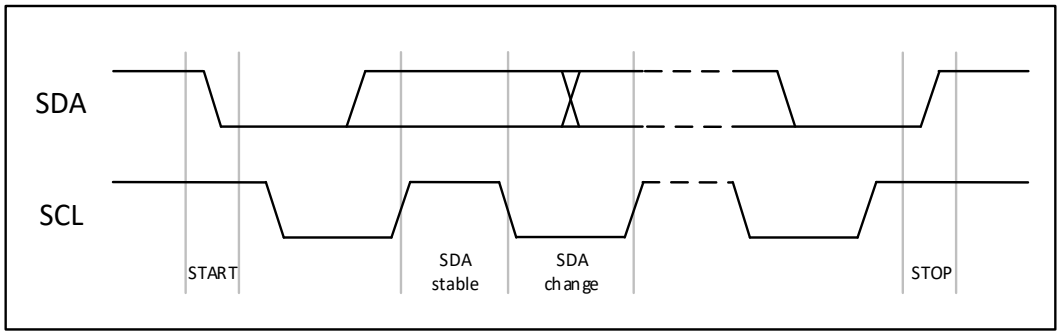



**Figure 2-10 : I²C START, STOP and data validity conditions**

The number of data bytes between the START and the STOP conditions is unlimited. Each byte of eight bits is followed by an acknowledge bit. After a START condition, the slave address combined with the R/W bit must be sent first. If the slave address corresponds to the device address, it will send an acknowledge bit by pulling down the SDA line and the data transfer is enabled. The I²C bus configurations for the read and write operations are shown in the following figures:

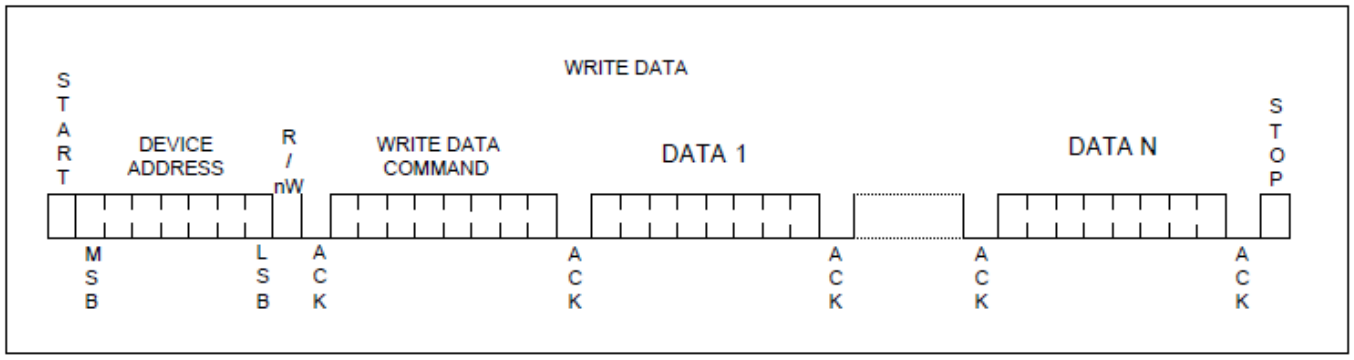



**Figure 2-11 : Write data transfer**

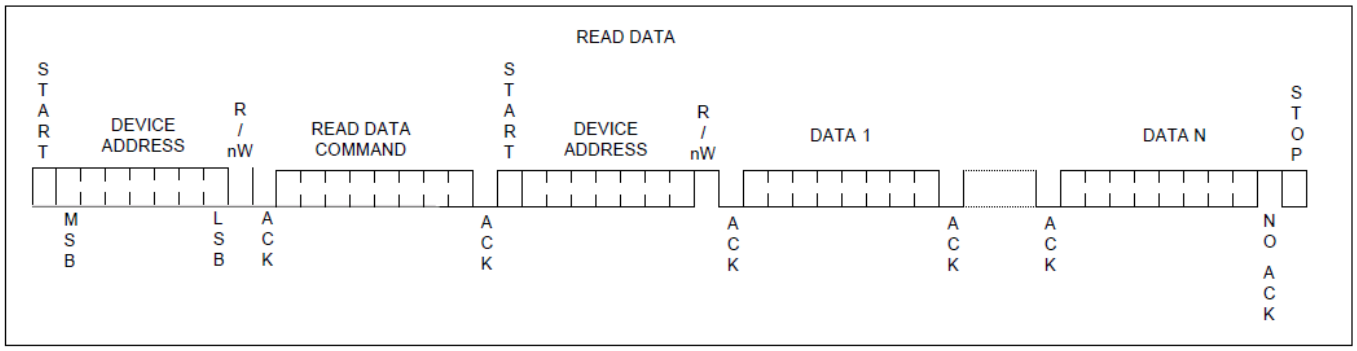



**Figure 2-12 : Read data transfer**

### 2.3.2. SPI INTERFACE

The SPI is a 4-wire interface. The nSS input is the control signal used to enable the device SPI interface. The clock signal SCK generated by the host synchronizes data transmission. The MOSI signal is the data input. The MISO signal is the data output and it is disabled by default; however, it can be enabled by software through the “en_MISO” bit in the configuration registers.

| EN | nSS | en_MISO bit | MISO |
|---|---|---|---|
| VSS | ‘x’ | ‘x’ | hi-Z |
| VDD | VDD | ‘x’ | hi-Z |
| VDD | VSS | ‘0’ | VSS |
| VDD | VSS | ‘1’ | Data |

**Table 2-15 : MISO pin status as a function of nSS and en_MISO**

When the device is disabled (EN = VSS) and the SPI interface is selected (CIS = VSS), the pin CIO2 (MISO signal) is in hi-Z state.

When nSS = VSS and en_MISO = ‘1’, the pin MISO outputs ‘0’ during write operations.

Three input pins allow to configure the SPI.

The CK_POL input selects the polarity of the SPI Clock:

- When set to VSS, the SCK clock signal is set to VSS between transmissions.
- When set to VDD, the SCK clock signal is set to VDD between transmissions.

The CK_PHA input pin selects the clock edge that samples data:

- When set to VSS, the data on MOSI input is sampled at the first edge of the SPI Clock.
- When set to VDD, the data on MOSI input is sampled at the second edge of the SPI Clock.

The MSB_FIRST input pin selects the ordering of the bits :

- When set to VSS, the bytes are sent LSB first.
- When set to VDD, the bytes are sent MSB first.

The SPI timing is shown in Figure 2-13, Figure 2-14, Figure 2-15 and Figure 2-16.

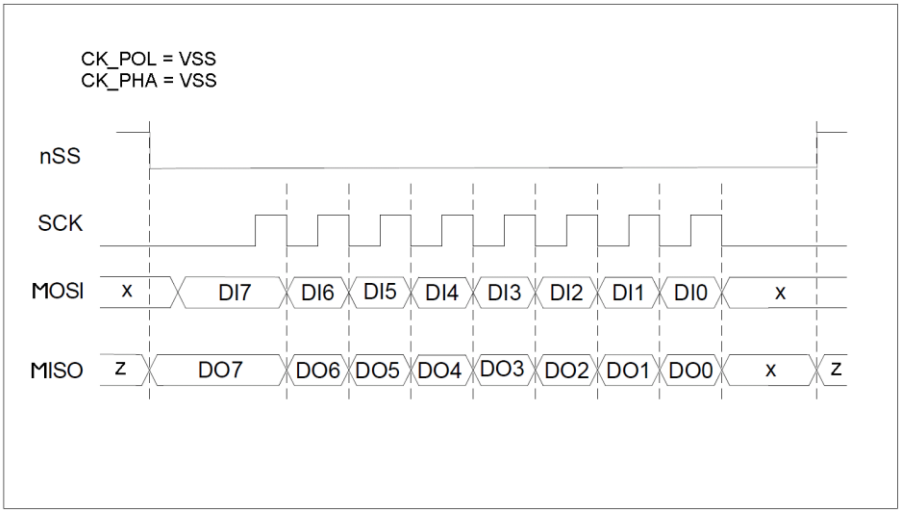



**Figure 2-13 : SPI timing with MSB_FIRST = VDD, CK_POL = VSS & CK_PHA = VSS**

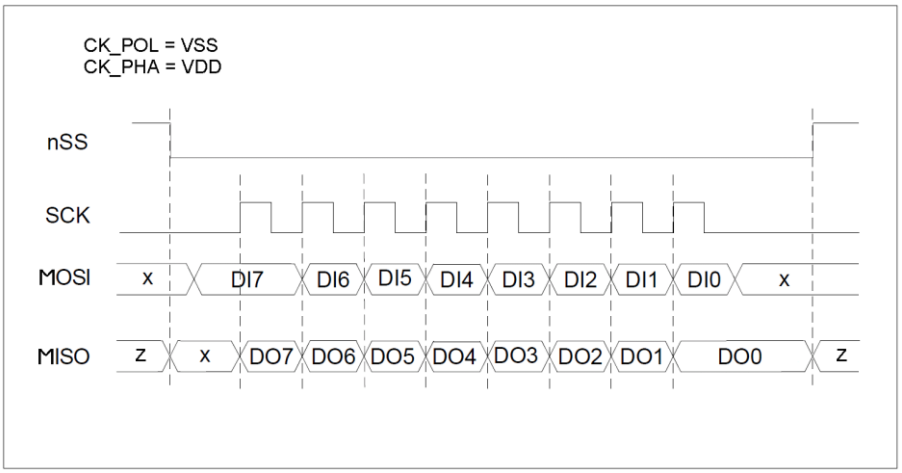



**Figure 2-14 : SPI timing with MSB_FIRST = VDD, CK_POL = VSS & CK_PHA = VDD**

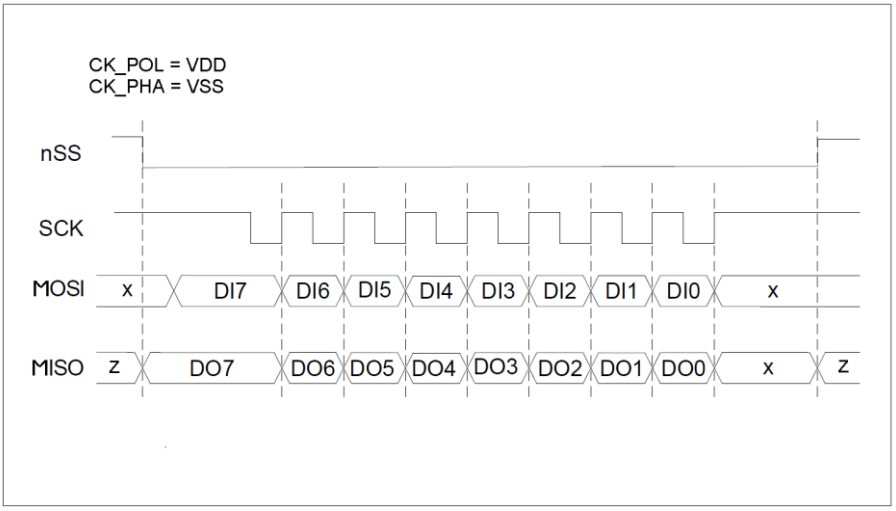



**Figure 2-15 : SPI timing with MSB_FIRST = VDD, CK_POL = VDD & CK_PHA = VSS**

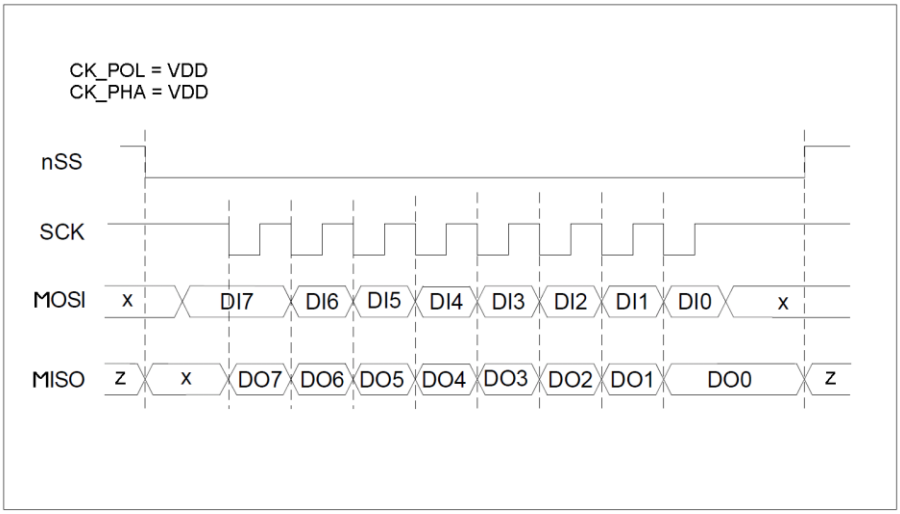



**Figure 2-16 : SPI timing with MSB_FIRST = VDD, CK_POL = VDD & CK_PHA = VDD**

## 2.4. COMMAND SET

The communication interface supports commands which enable to access the mapping dictionary and the registers. The first byte of a communication transfer is interpreted as a command. The commands are listed in the Table 2-16.

| Command | Opcode | Description |
|---|---|---|
| WRITE_REG | "0XXXXXXX" | Write internal registers at address XXXXXXX = $00 to $1F, $40 to $5F and $60 to $7F; the range $20 to $3F is not allowed. |
| READ_REG | "1XXXXXXX" | Read internal registers at address XXXXXXX = $00 to $1F; the range $20 to $7F is not allowed. See note [5]. |
| WRITE_DIC | "00100000" | Write dictionary with groups definition. Value = $20. |
| READ_DIC | "10100000" | Read dictionary with groups definition. Value = $A0. See note 5. |

**Table 2-16 : Command Set**

When the I²C interface is selected, the user shall take care of the consistency between the interface and the command directions (read or write):

- A "WRITE_" command must follow the I²C write data protocol (see Figure 2-11)

- A "READ_" command must follow the I²C read data protocol (see Figure 2-12)

- Any inconsistent access results in unpredictable behavior, for example an I²C read access with a "WRITE_REG" command.

## 2.5. RESET AND INITIALIZATION OF THE LCD SEGMENT DRIVER

The circuit is reset when it is powered on, when a brownout occurs during the active state or when the pin EN is set to VSS. If the reset is due to the power-on or a brownout, the MCU can detect it by two ways:

1. Through an interruption in the pin ICRDY. When a reset occurs, the ICRDY pin becomes inactive until the device is ready again to receive commands from the host. The polarity of the pin ICRDY is defined by the pin CI8/ICRDY_POL.

| CI8/ICRDY_POL | ICRDY | Device: |
|---|---|---|
| VSS | '0' | Ready |
| | '1' | Not ready |
| VDD | '0' | Not ready |
| | '1' | Ready |

**Table 2-17 : Meaning of ICRDY as a function of ICRDY_POL**

2. Reading the bit "Reset" in the command register. When a reset occurs, the bit "Reset" is set to '1'.

In harsh environments, it is strongly recommended to actively check for the reset occurrence.

After a reset, it is necessary to initialize the device. The following procedure is recommended:

1. If ICRDY is used, wait until the pin ICRDY is active. If ICRDY is not used, wait for the Communication interface start-up time (see subsection 3.7) and then check the bit "Reset" of the command register to '1', before writing it to '0'.
2. If necessary (see note 6), write the mapping dictionary with the definition of the LCD segments groups and the configuration registers with the following parameters: mux rate, frame frequency, $V_{REF}$ level, …
3. Enable the LCD using the "LCD_On" bit in the command register.

When LCD_On = '1', writing the mapping dictionary or many configuration registers is forbidden; the command and functional registers values can be modified.

[5] The commands READ_REG and READ_DIC have no effect in SPI mode if the MISO pin is disabled
[6] If the internal E²PROM is not used for the dictionary nor for the configuration registers initialization.

## 2.6. BLINK FUNCTION WITH MULTIPLE DRIVERS

When using the blink function with multiple EM6115 drivers, the blink clocks of each driver are not synchronized and it results in an irregular blinking. To avoid this problem, the I/O pin called BLK_CK enables to output the internal blink clock or to input an external clock.

Two bits in the configuration registers control the blink clock sharing: “Blk_Share” and “Blk_Master”. The bit “Blk_Share” enables the sharing function: if ‘0’, the BLK_CK pin is configured as an input with internal pulldown and has no effect; if ‘1’, the circuit can work as a master or as a slave depending on the value of the bit “Blk_Master”. When the bit “Blk_Master” is set to ‘1’, the circuit is master and BLK_CK is an output; when the bit “Blk_Master” is set to ‘0’, the circuit is slave and BLK_CK is an input.

Additionally, the master needs the bit “LCD_On” = ‘1’ to generate the blink clock.

It is recommended to configure the slave(s) first in order to avoid any signal conflict:

1. Slave(s): write ‘0’ to bit “Blk_Master” and ‘1’ to bit “Blk_Share”
2. Master: write ‘1’ to bit “Blk_Master” and ‘1’ to bit “Blk_Share”

In Figure 2-17, a typical application using two EM6115 drivers is shown. In this case, U1 is used as the master and U2 as the slave. The driver U1 outputs its internal blink clock and the driver U2 uses it instead of its own blink clock. This assures that the blinking is synchronous on both LCD drivers. Another possibility is to use both drivers as slaves and that a third circuit (not necessarily a driver) generates the blink clock. In this last case, the constraints on the BLK_CK input signal are as follows:

- BLK_CK signal level = ‘0’: the LCD segments are ON.
- BLK_CK signal level = ‘1’: the LCD segments are OFF.
- Minimum duration of each signal level, ‘0’ or ‘1’: one frame period (see chapter 2.7.2).
- Maximum frequency of BLK_CK signal: 10 Hz.

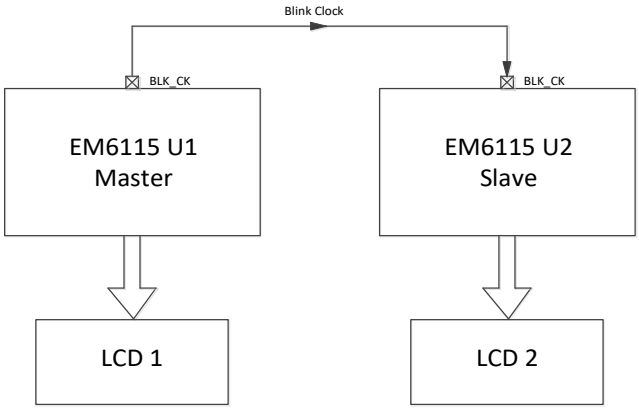



**Figure 2-17 : Connection of two drivers with synchronous blink function**

## 2.7. INTERNAL REGISTERS

| Function | Addr | Rst | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Cmd | $00 | $01 | R/W | WRITE_EE | DUMP_EE | - | Inverse | Blank | Blink | LCD_On | Reset |
| Password | $01 | $00 | R/W | Password [7:0] | | | | | | | |
| Reserved0 | $02 | - | - | - | - | - | - | - | - | - | - |
| … | ... | ... | … | ... | ... | ... | ... | ... | ... | ... | ... |
| Reserved16 | $12 | - | - | - | - | - | - | - | - | - | - |
| End_address | $13 | $0F | R/W | - | End_Addr [6:0] | | | | | | |
| Cfg0 | $14 | $00 | R/W | - | - | - | en_MISO | en_LowP | en_Bias3 | Mux [1:0] | |
| Cfg1 | $15 | $2C | R/W | - | - | Frame_Freq [2:0] | | | Vgen_Freq [2:0] | | |
| Cfg2 | $16 | $00 | R/W | Ident [5:0] | | | | | | Blk_Share | Blk_Master |
| Cfg3 | $17 | $08 | R/W | Blk_Freq [1:0] | | Vref_Level [5:0] | | | | | |
| en_Com | $18 | $FF | R/W | en_LCom4 | en_LCom3 | en_LCom2 | en_LCom1 | en_RCom4 | en_RCom3 | en_RCom2 | en_RCom1 |
| en_Seg [8:1] | $19 | $FF | R/W | en_Seg8 | en_Seg7 | en_Seg6 | en_Seg5 | en_Seg4 | en_Seg3 | en_Seg2 | en_Seg1 |
| en_Seg [16:9] | $1A | $FF | R/W | en_Seg16 | en_Seg15 | en_Seg14 | en_Seg13 | en_Seg12 | en_Seg11 | en_Seg10 | en_Seg9 |
| en_Seg [24:17] | $1B | $FF | R/W | en_Seg24 | en_Seg23 | en_Seg22 | en_Seg21 | en_Seg20 | en_Seg19 | en_Seg18 | en_Seg17 |
| en_Seg [32:25] | $1C | $FF | R/W | en_Seg32 | en_Seg31 | en_Seg30 | en_Seg29 | en_Seg28 | en_Seg27 | en_Seg26 | en_Seg25 |
| en_Seg [40:33] | $1D | $FF | R/W | en_Seg40 | en_Seg39 | en_Seg38 | en_Seg37 | en_Seg36 | en_Seg35 | en_Seg34 | en_Seg33 |
| en_Seg [48:41] | $1E | $FF | R/W | en_Seg48 | en_Seg47 | en_Seg46 | en_Seg45 | en_Seg44 | en_Seg43 | en_Seg42 | en_Seg41 |
| en_Seg [50:49] | $1F | $23 | R/W | - | - | - | - | - | - | en_Seg50 | en_Seg49 |
| Group0 | $40 | $00 | W | H0 | G0 | F0 | E0 | D0 | C0 | B0 | A0 |
| Group1 | $41 | $00 | W | H1 | G1 | F1 | E1 | D1 | C1 | B1 | A1 |
| … | ... | ... | … | ... | ... | ... | ... | ... | ... | ... | ... |
| Group31 | $5F | $00 | W | H31 | G31 | F31 | E31 | D31 | C31 | B31 | A31 |
| Blk_Gr0 | $60 | $00 | W | Blk_H0 | Blk_G0 | Blk_F0 | Blk_E0 | Blk_D0 | Blk_C0 | Blk_B0 | Blk_A0 |
| Blk_Gr1 | $61 | $00 | W | Blk_H1 | Blk_G1 | Blk_F1 | Blk_E1 | Blk_D1 | Blk_C1 | Blk_B1 | Blk_A1 |
| … | … | … | … | … | … | … | … | … | … | … | … |
| Blk_Gr31 | $7F | $00 | W | Blk_H31 | Blk_G31 | Blk_F31 | Blk_E31 | Blk_D31 | Blk_C31 | Blk_B31 | Blk_A31 |

**Table 2-18 : Internal registers**

The circuit is controlled by internal registers accessible via $I^2C$ or SPI. The registers are written with the command “WRITE_REG” which contains the register address. The first byte of the transfer is interpreted as the command and all the following byte(s) as register(s) value; notice that if the transfer contains more than one register value, the internal register address is automatically incremented after each register value. Within the specific address ranges $40 to $5F and $60 to $7F, the register address is automatically wrapped at the lowest address of this range; for example, the address $5F is followed by the address $40.

The greyed out registers can only be written when LCD_On = ‘0’.

Internal registers can be divided in four types:

1) Command register
2) Reserved, “Password” and “End_address” registers
3) Configuration registers
4) Functional registers

The “Password” and “End_address” registers are described in the chapter 2.8.

### 2.7.1. COMMAND REGISTER

| Function | Addr | Rst | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Cmd | $00 | $01 | R/W | WRITE_EE | DUMP_EE | - | Inverse | Blank | Blink | LCD_On | Reset |

**Table 2-19 : Command register**

**Inverse:** in inverse mode the OFF LCD segments become ON and the ON segments become OFF.

**Blank:** sets OFF all the LCD segments.

**Blink:** global blink of all LCD segments. It has priority over the individual blink selected by bits “Blk_GrX” in the functional registers.

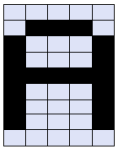
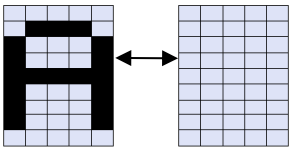
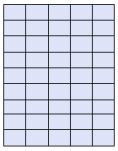
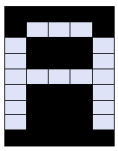
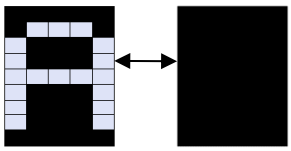
| Inverse | Blank | Blink | Display |
|---|---|---|---|
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  Alternating display |
| 0 | 1 | X |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  Alternating display |
| 1 | 1 | X |  |

**Table 2-20 : Combinations of Inverse, Blank & Blink modes**

**LCD_On**: when ‘1’ the circuit drives the LCD. When ‘0’ the circuit enters in a low power state, but the content of the internal registers is maintained.

**Reset**: this bit indicates that a reset event occurred (bit value is ‘1’). If the user wants to detect further reset events, the bit should be cleared by writing it to ‘0’.

**WRITE_EE & DUMP_EE**: both bits can be accessed in engineering mode only.

## 2.7.2. CONFIGURATION REGISTERS

| Function | Addr | Rst | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Cfg0 | $14 | $00 | R/W | - | - | - | en_MISO | en_LowP | en_Bias3 | Mux [1:0] | |
| Cfg1 | $15 | $2C | R/W | - | - | Frame_Freq [2:0] | | | Vgen_Freq [2:0] | | |
| Cfg2 | $16 | $00 | R/W | Ident [5:0] | | | | | | Blk_Share | Blk_Master |
| Cfg3 | $17 | $08 | R/W | Blk_Freq[0:1] | | Vref_Level [5:0] | | | | | |
| en_Com | $18 | $FF | R/W | en_LCom4 | en_LCom3 | en_LCom2 | en_LCom1 | en_RCom4 | en_RCom3 | en_RCom2 | en_RCom1 |
| en_Seg [8:1] | $19 | $FF | R/W | en_Seg8 | en_Seg7 | en_Seg6 | en_Seg5 | en_Seg4 | en_Seg3 | en_Seg2 | en_Seg1 |
| en_Seg [16:9] | $1A | $FF | R/W | en_Seg16 | en_Seg15 | en_Seg14 | en_Seg13 | en_Seg12 | en_Seg11 | en_Seg10 | en_Seg9 |
| en_Seg [24:17] | $1B | $FF | R/W | en_Seg24 | en_Seg23 | en_Seg22 | en_Seg21 | en_Seg20 | en_Seg19 | en_Seg18 | en_Seg17 |
| en_Seg [32:25] | $1C | $FF | R/W | en_Seg32 | en_Seg31 | en_Seg30 | en_Seg29 | en_Seg28 | en_Seg27 | en_Seg26 | en_Seg25 |
| en_Seg [40:33] | $1D | $FF | R/W | en_Seg40 | en_Seg39 | en_Seg38 | en_Seg37 | en_Seg36 | en_Seg35 | en_Seg34 | en_Seg33 |
| en_Seg [48:41] | $1E | $FF | R/W | en_Seg48 | en_Seg47 | en_Seg46 | en_Seg45 | en_Seg44 | en_Seg43 | en_Seg42 | en_Seg41 |
| en_Seg [50:49] | $1F | $23 | R/W | - | - | - | - | - | - | en_Seg50 | en_Seg49 |

**Table 2-21 : Configuration registers**

The configuration registers from the address $14 to $15 can only be written when the bit “LCD_On” = ‘0’.

**en_MISO:** when ‘1’ the MISO pin is enabled. When ‘0’ it is disabled and outputs VSS (see Table 2-15).

**en_LowP:** selects either the Normal or Low Power mode when Mux2, Mux3 or Mux4 are used.

| en_LowP | Mode |
|---|---|
| 0 | Normal |
| 1 | Low power |

**en_Bias3:** selects the biasing scheme when Mux2, Mux3 or Mux4 addressing are used.

| en_Bias3 | Bias |
|---|---|
| 0 | ½ |
| 1 | ⅓ |

**en_LowP & en_Bias3:** define the $V_{ON}$ voltage used in static addressing.

| en_LowP | en_Bias3 | Static $V_{ON}$ |
|---|---|---|
| 0 | 0 | 2 x $V_{REF}$ |
| 0 | 1 | $V_{REF}$ |
| 1 | 0 | $V_{REF}$ / 2 |
| 1 | 1 | 3 x $V_{REF}$ |

**Mux [1:0]:** sets the addressing mode (mux) of the driver.

| Mux [1:0] | Addressing |
|---|---|
| 00 | Static |
| 01 | Mux2 |
| 10 | Mux3 |
| 11 | Mux4 |

**Frame_Freq [2:0]:** sets the frame rate frequency.

| Frame_Freq [2:0] | Freq (Hz) | | | |
|---|---|---|---|---|
| | Static | Mux2 | Mux3 | Mux4 |
| 000 | 5.33 | 5.33 | 5.33 | 5.33 |
| 001 | 8 | 8 | 8.53 | 8 |
| 010 | 10.67 | 10.67 | 10.67 | 10.67 |
| 011 | 16 | 16 | 17.07 | 16 |
| 100 | 21.33 | 21.33 | 21.33 | 21.33 |
| 101 | 32 | 32 | 34.13 | 32 |
| 110 | 42.67 | 42.67 | 42.67 | 42.67 |
| 111 | 64 | 64 | 68.27 | 64 |

**Vgen_Freq [2:0]**: sets the clock frequency for the charge pumps in the voltage generator. It should be adapted to the effective load current: the higher the frequency, the higher the load current, as shown in the following table. See also the section 2.9.5 for further details.

| Vgen_Freq [2:0] | Charge Pumps Freq (Hz) | Recommended IDD with LCD connected (µA) |
|---|---|---|
| 000 | 64 | 0.20 |
| 001 | 128 | 0.30 |
| 010 | 256 | 0.45 |
| 011 | 512 | 0.75 |
| 100 | 1024 | 1.3 |
| 101 | 2048 | 2.5 |
| 110 | 4096 | 5.0 |
| 111 | 8192 | 10.0 |

**Ident [5:0]:** reserved for the device identification. The default value is $00.

**Blk_Share:** enable of the blink clock sharing. When '1' the circuit can work as a master or as a slave depending on the value of the bit "Blk_Master". When '0' the BLK_CK pin is configured as input with internal pulldown. When the pin EN = VSS, the BLK_CK pin is also configured as input with internal pulldown.

**Blk_Master:** used when the blink clock sharing is enabled. When '0' the circuit is in slave mode. When '1' the circuit is in master mode. Warning: take care to avoid any signal conflict when configured in master mode.

**Blink_Freq [1:0]:** sets the blinking frequency. The blinking frequency must be at most half of the frame frequency; both individual and global blink functions use the same frequency. The blink duty cycle is 50%. The change of blink frequency while blink is enabled can cause an artefact in the next blink period.

| Blink_Freq [1:0] | Freq (Hz) |
|---|---|
| 00 | 0.5 |
| 01 | 1 |
| 10 | 2 |
| 11 | 4 |

**Vref_Level [5:0]**: sets the voltage reference level, $V_{REF}$ (V) = 0.8 + 0.025 x Vref_Level. Depending on the selected circuit settings, the range Vref_Level = [0, 63] can be not fully valid (see sections 2.1.3, 2.1.4 and 2.1.5).

**en_LCom [4:1], en_RCom [4:1]**: there are different possibilities to output COM lines: at the left, at the right or at both sides of the SEG lines. A disabled COM line outputs VSS and shall not be connected to any physical LCD plane.

| Bits | Description |
|---|---|
| en_LCom [4:1] | Left side LCOM [4:1] pin individual enable |
| en_RCom [4:1] | Right side RCOM [4:1] pin individual enable |

**en_Seg [50:1]:** enable for each of the 50 SEG lines. All disabled SEG lines are set at VSS for power saving and shall not be connected to any physical LCD segment.

### 2.7.3. FUNCTIONAL REGISTERS

| Function | Addr | Rst | R/W | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Group0 | $40 | $00 | W | H0 | G0 | F0 | E0 | D0 | C0 | B0 | A0 |
| Group1 | $41 | $00 | W | H1 | G1 | F1 | E1 | D1 | C1 | B1 | A1 |
| … | ... | ... | … | ... | ... | ... | ... | ... | ... | ... | ... |
| Group31 | $5F | $00 | W | H31 | G31 | F31 | E31 | D31 | C31 | B31 | A31 |
| Blk_Gr0 | $60 | $00 | W | Blk_H0 | Blk_G0 | Blk_F0 | Blk_E0 | Blk_D0 | Blk_C0 | Blk_B0 | Blk_A0 |
| Blk_Gr1 | $61 | $00 | W | Blk_H1 | Blk_G1 | Blk_F1 | Blk_E1 | Blk_D1 | Blk_C1 | Blk_B1 | Blk_A1 |
| … | … | … | … | … | … | … | … | … | … | … | … |
| Blk_Gr31 | $7F | $00 | W | Blk_H31 | Blk_G31 | Blk_F31 | Blk_E31 | Blk_D31 | Blk_C31 | Blk_B31 | Blk_A31 |

**Table 2-22 : Functional registers**

These registers are “write-only” and any read operation at their addresses returns meaningless values.

**GroupX:** when ‘1’, switches ON the corresponding LCD segments within a group, according to their definition in the mapping dictionary.

**Blk_GrX:** when ‘1’, enables the blink of the corresponding LCD segments within a group. The definition of groups is the same as that used in the registers GroupX (defined in the mapping dictionary). Only the LCD segments that are switched ON can blink.

## 2.8. ENGINEERING MODE

The engineering mode unlocks the EEPROM access under specific conditions. This 128x16 EEPROM memory can be useful at the reset of the circuit, as it is automatically dumped to the internal registers and the mapping dictionary. By this way, the host does not need to write the configuration registers nor the mapping dictionary and the circuit is completely functional after startup.

### 2.8.1. ACCESS AND FUNCTIONS OF THE ENGINEERING MODE

| Function | Addr | Rst | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|
| Cmd | $00 | $01 | WRITE_EE | DUMP_EE | - | Inverse | Blank | Blink | LCD_On | Reset |
| Password | $01 | $00 | Password [7:0] | | | | | | | |
| End_address | $13 | $0F | - | End_Addr [6:0] | | | | | | |

**Table 2-23 : Relevant registers for the Engineering mode**

This mode is accessed by the password (value = $AC) written to the internal register “Password”. The engineering mode does not allow access to individual addresses of the EEPROM for writing or reading, but considers a block of data ending at the EEPROM address End_Addr[6:0]. This value can only be written to the register “End_address” when the bit “LCD_On” = ‘0’; the valid values are $09 to $7F. It is strongly recommended to reset the password value after the completion of an EEPROM operation to avoid unwanted effects.

As can be seen in Table 2-24 : EEPROM operations , the register “Cmd” gets two functional bits, “WRITE_EE” and “DUMP_EE” that can be accessed only in engineering mode. These bits can be set to start an EEPROM operation, and they are automatically reset after completion; however, the operation’s completion cannot be checked with these bits, as the communication interface is disabled during the EEPROM operation. The end of the EEPROM operation is only signaled by the state of the ICRDY pin (see Chapter 2.5 for the pin polarity setting), or by waiting for a given delay ($t_{WRITE\_EE}$ and $t_{DUMP\_EE}$ in Table 3-1). Both bits “WRITE_EE” and “DUMP_EE” can only be written when the bit “LCD_On” = ‘0’.

| WRITE_EE | DUMP_EE | Description | Last EEPROM address accessed |
|---|---|---|---|
| 0 | 1 | Dump content of EEPROM to internal registers and mapping dictionary | End_Addr [6:0] written in EEPROM |
| 1 | X | Copy content of internal registers and mapping dictionary to EEPROM | End_Addr [6:0] written in register “End_address” |

**Table 2-24 : EEPROM operations**

### 2.8.2. EEPROM READ OPERATION

In order to read the internal EEPROM, the steps are as follows:

1. Disable the LCD driver: reset bit “LCD_On” in the register “Cmd”.
2. Unlock the Engineering Mode: write the password value ($AC) to the register “Password”.
3. Set the bit “DUMP_EE” in the register “Cmd”.
4. Check the ICRDY pin or wait for the delay $t_{DUMP\_EE}$.
5. Lock the Engineering Mode: write the value $00 to the register “Password”.

### 2.8.3. EEPROM WRITE OPERATION

In order to write the internal EEPROM, the steps are as follows:

1. Disable the LCD driver: reset bit “LCD_On” in the register “Cmd”.
2. Set the VDD pin to $VDD_{WR}$ value.
3. Write the desired data to the configuration registers and the dictionary, and then update the register “End_address” with the desired last EEPROM address to be written.
4. Unlock the Engineering Mode: write the password value ($AC) to the register “Password”.
5. Set the bit “WRITE_EE” in the register “Cmd”.
6. Check the ICRDY pin or wait for the delay $t_{WRITE\_EE}$.
7. Lock the Engineering Mode: write the value $00 to the register “Password”.

Warning: any interruption of external supply during write operation can induce an error. In that case, the user should repeat the operation again.

## 2.8.4. EEPROM CORRESPONDENCE TO INTERNAL REGISTERS AND DICTIONARY

The content of the internal registers (from $14 to $1F) are stored at the addresses $0A to $0F of the 128X16 EEPROM, and the mapping dictionary is stored at the addresses $10 to $73. The format is as follows (yellow = configuration registers; green = mapping dictionary):

| Function | Addr | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| - | $00 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| Reserved1 & Reserved0 | $01 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … |
| End_address& Reserved16 | $09 | - | End_Addr [6:0] | | | | | | | - | - | - | - | - | - | - | - |
| Cfg1 & Cfg0 | $0A | - | - | Frame_Freq [2:0] | | | Vgen_Freq [2:0] | | | - | - | - | en_MISO | en_LowP | en_Bias3 | Mux [1:0] | |
| Cfg3 & Cfg2 | $0B | Blk_Freq [1:0] | | Vref_Level [5:0] | | | | | | Ident [5:0] | | | | | | Blk_Share | Blk_Master |
| en_Seg[8:1] & en_Com[4:1] | $0C | en_Seg8 | en_Seg7 | en_Seg6 | en_Seg5 | en_Seg4 | en_Seg3 | en_Seg2 | en_Seg1 | en_LCom4 | en_LCom3 | en_LCom2 | en_LCom1 | en_RCom4 | en_RCom3 | en_RCom2 | en_RCom1 |
| en_Seg [24:9] | $0D | en_Seg24 | en_Seg23 | en_Seg22 | en_Seg21 | en_Seg20 | en_Seg19 | en_Seg18 | en_Seg17 | en_Seg16 | en_Seg15 | en_Seg14 | en_Seg13 | en_Seg12 | en_Seg11 | en_Seg10 | en_Seg9 |
| en_Seg [40:25] | $0E | en_Seg40 | en_Seg39 | en_Seg38 | en_Seg37 | en_Seg36 | en_Seg35 | en_Seg34 | en_Seg33 | en_Seg32 | en_Seg31 | en_Seg30 | en_Seg29 | en_Seg28 | en_Seg27 | en_Seg26 | en_Seg25 |
| en_Seg [50:41] | $0F | - | - | - | - | - | - | en_seg50 | en_Seg49 | en_Seg48 | en_Seg47 | en_Seg46 | en_Seg45 | en_Seg44 | en_Seg43 | en_Seg42 | en_Seg41 |
| SEG1 : COM2 & COM1 | $10 | Ngrp_012[4:0] | | | | | Nbit_012[2:0] | | | Ngrp_011[4:0] | | | | | Nbit_011[2:0] | | |
| SEG1 : COM4 & COM3 | $11 | Ngrp_014[4:0] | | | | | Nbit_014[2:0] | | | Ngrp_013[4:0] | | | | | Nbit_013[2:0] | | |
| SEG2 : COM2 & COM1 | $12 | Ngrp_022[4:0] | | | | | Nbit_022[2:0] | | | Ngrp_021[4:0] | | | | | Nbit_021[2:0] | | |
| … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … |
| SEG50 : COM4 & COM3 | $73 | Ngrp_504[4:0] | | | | | Nbit_504[2:0] | | | Ngrp_503[4:0] | | | | | Nbit_503[2:0] | | |
| - | $74 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … |
| - | $7F | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

**Table 2-25 : EEPROM correspondence to internal registers and dictionary**

## 2.9. ANALOG SYSTEM FUNCTIONS

### 2.9.1. VOLTAGE REGULATOR

The regulated voltage $V_{REG}$ is connected to the following blocks: logic, internal registers, oscillator, EEPROM and POR. The voltage $V_{REG}$ is available at the pin VREG, where the capacitor $C_{VREG}$ must be connected to implement the filter function. The nominal value of $V_{REG}$ is 1.05 V; as the VDD supply voltage approaches 1.0 V, the internal voltage regulator becomes a voltage follower with a minimum voltage drop.

The $C_{VREG}$ capacitor nominal value is 1µF. The capacitor should be of type MLCC (Multi-Layer Ceramic Typ II).

### 2.9.2. POWER ON RESET

The POR senses the regulated voltage $V_{REG}$. The cell has two functions:

1. It triggers a system reset after the voltage regulator is switched on. The POR produces a reset until the end of the POR delay, after $V_{REG}$ becomes higher than the threshold voltage $V_{POR}$. The delay is long enough to assure the correct reset of all the registers in the circuit.
2. It monitors the regulated voltage and initiate a system reset if $V_{REG}$ drops below the threshold voltage $V_{POR}$. This threshold is defined to a value which is below the specified regulated voltage range, but high enough to ensure that all the registers can maintain their states.

### 2.9.3. OSCILLATOR

The circuit has an internal 8.2 kHz RC oscillator. The necessary clock signals for the voltage generator and for the LCD waveforms generator are obtained through programmable prescalers.

### 2.9.4. VOLTAGE REFERENCE

The device has an on-chip voltage reference which determines the voltage level of the LCD waveforms. The voltage reference is programmable with the register “Vref_Level” and can therefore be adapted to different LCD module characteristics.

### 2.9.5. VOLTAGE GENERATOR

To generate the necessary voltage levels VL1, VL2 and VL3, the driver is equipped with a voltage generator based on two charge pumps. The charge pumps frequency is programmable (“Vgen_Freq”) and should be adapted to the current consumption of the display. If the frequency is too low for a given load current, the generated voltages will be lower than expected, and this can result in a DC offset voltage on the LCD segments. It is strongly recommended to control the generated voltages with the display connected to the circuit.

External capacitors (100 nF and 1 uF nominal value) are needed and should be of type MLCC (Multi-Layer Ceramic Typ II).

Depending on the selected circuit settings, $C_{VL1}$ or $C_{VL2}$ need a capacitor with a nominal value of 1 µF (see sections 2.1.2 and 2.1.3). The effective capacitance of the 1 µF capacitor can affect the stability of the circuit because the capacitor is used by the voltage reference. Stability is ensured with an effective capacitance of 300 nF or higher. The effective capacitance refers to the capacitance after taking into account the tolerance, the bias voltage derating and the temperature derating of the capacitor. Using a capacitor with a nominal value of 300 nF does not ensure stability because the effective capacitance under the operating conditions must not be less than 300 nF.

All other capacitors in the voltage generator have a nominal value of 100 nF. These 100 nF capacitors do not affect the stability of the circuit because they are used by the charge pumps. Therefore, there are no special requirements for their effective capacitance.

# 3. ELECTRICAL SPECIFICATIONS

## 3.1. ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Storage temperature | $T_{STORE}$ | | -40 | 125 | °C |
| Supply voltage | VDD | VSS = 0 V | -0.2 | 3.6 | V |
| Voltage on any pin | $V_{MAX}$ | | VSS-0.2 | VDD+0.2 | V |
| $V_{ESD}$ | ESD Voltage | HBM Note [7] | | ±2000 | V |
| $I_{LU}$ | Latch-up Current | Jedec Note [8] | | ±100 | mA |

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

## 3.2. HANDLING PROCEDURES

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

## 3.3. OPERATING CONDITIONS

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating temperature | $T_{OP}$ | | -40 | | 85 | °C |
| Supply voltage range | VDD | | 1.0 | | 3.6 | V |
| Reference terminal | VSS | | | 0 | | V |
| Regulator capacitor | $C_{VREG}$ | | | 1 | | µF |

## 3.4. ELECTRICAL CHARACTERISTICS AT VDD=3V

Operating conditions unless otherwise specified: VDD = 3 V, T = 25°C

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Supply current: disable | $IDD_{DIS}$ | EN = VSS | | | | 10 | nA |
| Supply current: LCD OFF | $IDD_{OFF}$ | EN = VDD, LCD_On = '0' | | | 50 | | nA |
| Supply current: normal mode | $IDD_{NM}$ | Note [9] | Vref_Level = $08 | | 150 | | nA |
| Supply current: low power mode | $IDD_{LP}$ | | Vref_Level = $30 | | 130 | | nA |

[7] HBM: Human Body Model according to JS-001.
[8] Latch-up testing according to JESD78 Class I (room temperature) level A (100 mA)
[9] Mux2; Bias ½; without LCD display; 50% LCD segments ON; Frame_Freq = $05; Vgen_Freq = $02

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Input Pins** | | | | | | | |
| Low level input voltage | $V_{IL}$ | | | | | 0.3xVDD | V |
| High level input voltage | $V_{IH}$ | | | 0.7xVDD | | | V |
| Input leakage | $I_{IN}$ | $V_{IN}$ = VSS or VDD | | -100 | | 100 | nA |
| **LCD Pins** | | | | | | | |
| COM Low level output current | $I_{OL\_COM}$ | VL3=3V | $V_{OUT}$ = 50 mV | | | -400 | µA |
| COM High level output current | $I_{OH\_COM}$ | | $V_{OUT}$ = VL3 - 50 mV | 200 | | | µA |
| SEG Low level output current | $I_{OL\_SEG}$ | | $V_{OUT}$ = 50 mV | | | -60 | µA |
| SEG High level output current | $I_{OH\_SEG}$ | | $V_{OUT}$ = VL3 - 50 mV | 30 | | | µA |
| **Regulator** | | | | | | | |
| Regulator Voltage | $V_{REG}$ | 10 µA load | | 1.00 | 1.05 | 1.10 | V |
| **Power-On-Reset at $V_{REG}$** | | | | | | | |
| Threshold Voltage | $V_{POR}$ | | | 0.70 | 0.80 | 0.90 | V |
| **RC Oscillator** | | | | | | | |
| Frequency | $F_{RC}$ | | | 8.0 | 8.2 | 8.4 | kHz |
| **LCD Driver** | | | | | | | |
| Voltage Level 1 | VL1 | Note [10] | Vref_Level = $00 | | 0.800 | | V |
| | | | Vref_Level = $01 | | 0.825 | | |
| | | | Vref_Level = $02 | | 0.850 | | |
| | | | Vref_Level = $04 | | 0.900 | | |
| | | | Vref_Level = $08 | -1.5% | 1.000 | +1.5% | |
| | | | Vref_Level = $10 | | 1.200 | | |
| | | | Vref_Level = $20 | | 1.600 | | |
| | | | Vref_Level = $3F | | 2.375 | | |
| VL1 temperature dependency | ΔVL1/ΔT | | Vref_Level = $08 | | -200 | | ppm/°C |
| VL1 voltage dependency | ΔVL1/ΔVDD | | Vref_Level = $08; VDD = 1.1 to 3.6 V | | 1.4 | | mV/V |

[10] 1 µA load; Static Drive, $V_{ON}$ = $V_{REF}$; SEGs and COMs disabled

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage Level 2 | VL2 | Note [11] | 1 uA load in VL2<br>1 uA load in VL3 | 2 x $VL1_{MIN}$ - 30 mV | 2 x VL1 | 2 x $VL1_{MAX}$ + 30 mV | V |
| Voltage Level 3 | VL3 | | | 3 x $VL1_{MIN}$ - 45 mV | 3 x VL1 | 3 x $VL1_{MAX}$ + 45 mV | V |
| DC Voltage | $V_{DC}$ | Note [12] | | | | 50 | mV |

## 3.5. ELECTRICAL CHARACTERISTICS AT VDD=1.55V

Operating conditions unless otherwise specified: VDD = 1.55 V, T = 25°C

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Supply current: disable | $IDD_{DIS}$ | EN = VSS | | | | 10 | nA |
| Supply current: LCD OFF | $IDD_{OFF}$ | EN = VDD, LCD_On = '0' | | | 50 | | nA |
| Supply current: normal mode | $IDD_{NM}$ | Note [13] | Vref_Level = $08 | | 150 | | nA |
| **Input Pins** | | | | | | | |
| Low level input voltage | $V_{IL}$ | | | | | 0.3xVDD | V |
| High level input voltage | $V_{IH}$ | | | 0.7xVDD | | | V |
| Input leakage | $I_{IN}$ | $V_{IN}$ = VSS or VDD | | -100 | | 100 | nA |
| **LCD Pins** | | | | | | | |
| COM Low level output current | $I_{OL\_COM}$ | VL3=3V | $V_{OUT}$ = 50 mV | | | -400 | µA |
| COM High level output current | $I_{OH\_COM}$ | | $V_{OUT}$ = VL3 - 50 mV | 200 | | | µA |
| SEG Low level output current | $I_{OL\_SEG}$ | | $V_{OUT}$ = 50 mV | | | -60 | µA |
| SEG High level output current | $I_{OH\_SEG}$ | | $V_{OUT}$ = VL3 - 50 mV | 30 | | | µA |
| **Regulator** | | | | | | | |
| Regulator Voltage | $V_{REG}$ | 10 µA load | | 1.00 | 1.05 | 1.10 | V |
| **Power-On-Reset at $V_{REG}$** | | | | | | | |
| Threshold Voltage | $V_{POR}$ | | | 0.70 | 0.80 | 0.90 | V |
| **RC Oscillator** | | | | | | | |

[11] Vref_Level = $08; Vgen_Freq = $07; SEGs and COMs disabled; Normal mode, Bias ⅓
[12] Average voltage measured between any SEG and COM outputs, over a whole frame period
[13] Mux2; Bias ½; without LCD display; 50% LCD segments ON; Frame_Freq = $05; Vgen_Freq = $02

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Frequency | $F_{RC}$ | | 8.0 | 8.2 | 8.4 | kHz |

Operating conditions unless otherwise specified: VDD = 1.55 V, T = 25°C

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **LCD Driver** | | | | | | | |
| Voltage Level 1 | VL1 | Note [14] | Vref_Level = $00 | | 0.800 | | V |
| | | | Vref_Level = $01 | | 0.825 | | |
| | | | Vref_Level = $02 | | 0.850 | | |
| | | | Vref_Level = $04 | | 0.900 | | |
| | | | Vref_Level = $08 | -1.5% | 1.000 | +1.5% | |
| | | | Vref_Level = $10 | | 1.200 | | |
| VL1 temperature dependency | ΔVL1/ΔT | | Vref_Level = $08 | | -200 | | ppm/°C |
| VL1 voltage dependency | ΔVL1/ΔVDD | | Vref_Level = $08; VDD = 1.1 to 3.6 V | | 1.4 | | mV/V |
| Voltage Level 2 | VL2 | Note [15] | 1 uA load in VL2<br>1 uA load in VL3 | $2 \times VL1_{MIN}$ - 30 mV | 2 x VL1 | $2 \times VL1_{MAX}$ + 30 mV | V |
| Voltage Level 3 | VL3 | | | $3 \times VL1_{MIN}$ - 45 mV | 3 x VL1 | $3 \times VL1_{MAX}$ + 45 mV | V |
| DC Voltage | $V_{DC}$ | Note [16] | | | | 50 | mV |

## 3.6. EEPROM ACCESS – SPECIFICATIONS

**Operating conditions unless otherwise specified: VDD = 3 V, T = 25°C**

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating temperature in EEPROM write | $T_{WR}$ | | -10 | 25 | 60 | °C |
| VDD range for valid EEPROM write | $VDD_{WR}$ | | 1.4 | | 3.6 | V |
| $V_{REG}$ during EEPROM write | $V_{REG\_WR}$ | 10 µA load | 1.04 | 1.14 | 1.24 | V |
| Delay for complete EEPROM write (WRITE_EE) | $t_{WRITE\_EE}$ | | | 700 | 1000 | ms |
| Delay for complete EEPROM read (DUMP_EE) | $t_{DUMP\_EE}$ | | | 10 | 12 | ms |
| Writing endurance | $n_{CYC}$ | | 1000 | | | cycles |

**Table 3-1 : EEPROM access specifications**

[14] 1 µA load; Static Drive, $V_{ON} = V_{REF}$; SEGs and COMs disabled
[15] Vref_Level = $08; Vgen_Freq = $07; SEGs and COMs disabled; Normal mode, Bias ⅓
[16] Average voltage measured between any SEG and COM outputs, over a whole frame period

## 3.7. TIMING CHARACTERISTICS

Operating conditions unless otherwise specified: VDD = 1.55 & 3 V, T = 25°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Communication interface Start-up time | $t_{ST}$ | Note [17] | | | 25 | ms |
| Device disable time | $t_{DIS}$ | Note [18] | 50 | | | ms |
| **I²C** | | | | | | |
| SCL frequency | $f_{SCL}$ | | | 100 | 400 | kHz |
| SCL low period | $t_{LOW}$ | | 1.3 | | | µs |
| SCL high period | $t_{HIGH}$ | | 600 | | | ns |
| SDA setup time | $t_{SU;DAT}$ | | 100 | | | ns |
| SDA hold time | $t_{HD;DAT}$ | | 0 | | 900 | ns |
| SCL and SDA rise time | $t_R$ | | 20 | | 300 | ns |
| SCL and SDA fall time | $t_F$ | | | | 300 | ns |
| Setup time for a repeated start condition | $t_{SU;STA}$ | | 600 | | | ns |
| Hold time for a start condition | $t_{HD;STA}$ | | 600 | | | ns |
| Setup time for a stop condition | $t_{SU;STO}$ | | 600 | | | ns |
| Spike width on SCL and SDA | $t_{SP}$ | | | | 50 | ns |
| Time before a new transmission can start | $t_{BUF}$ | | 1.3 | | | µs |
| **SPI** | | | | | | |
| SCK frequency | $f_{SPI}$ | | | | 500 | kHz |
| SCK low period | $t_{SCL}$ | | 900 | | | ns |
| SCK high period | $t_{SCH}$ | | 900 | | | ns |
| SCK rise time | $t_{SCR}$ | | | | 100 | ns |
| SCK fall time | $t_{SCF}$ | | | | 100 | ns |
| MOSI setup time | $t_{MOSU}$ | | 250 | | | ns |
| MOSI hold time | $t_{MOH}$ | | 50 | | | ns |
| MISO hold time | $t_{MIH}$ | | | | 0 | ns |

[17] The communication interface is ready when the pin ICRDY is active. If ICRDY is not used, the given time must be respected.
[18] After disabling the device (pin EN = VSS), a delay must be respected before re-enabling it (pin EN = VDD).

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| MISO delay out | $t_{MIDO}$ | | | | 250 | ns |
| MISO delay Z | $t_{MIDZ}$ | | | | 250 | ns |
| nSS setup time | $t_{nSSSU}$ | | 1.0 | | | µs |
| nSS hold time | $t_{nSSH}$ | | 250 | | | ns |
| nSS high time (Bus free time between communication frames) | $t_{SPBUF}$ | | 1.5 | | | µs |

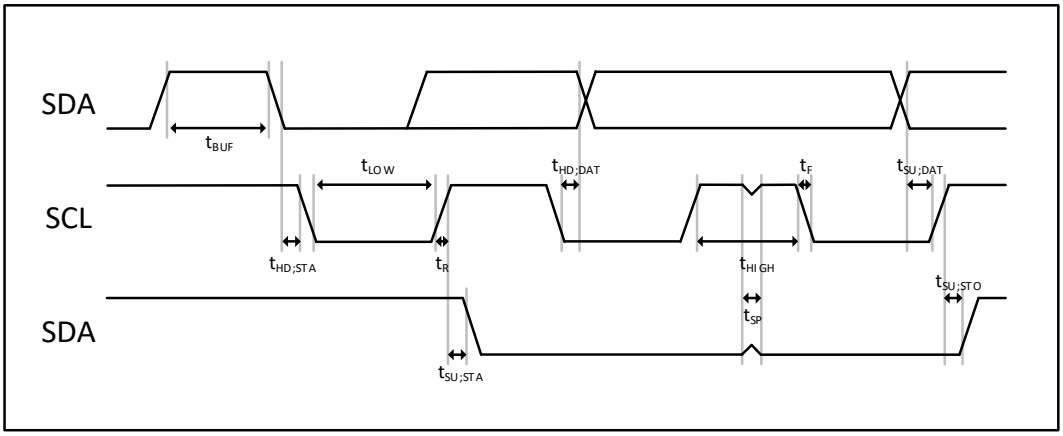



**Figure 3-1 : I2C timing characteristics**

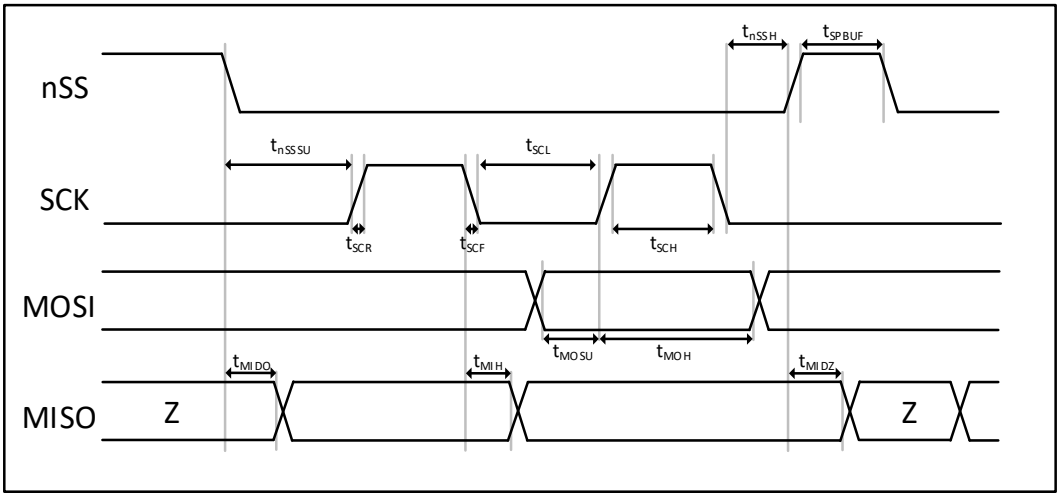



**Figure 3-2 : SPI timing characteristics with CK_POL = VSS & CK_PHA = VSS**

## 4. TYPICAL APPLICATIONS

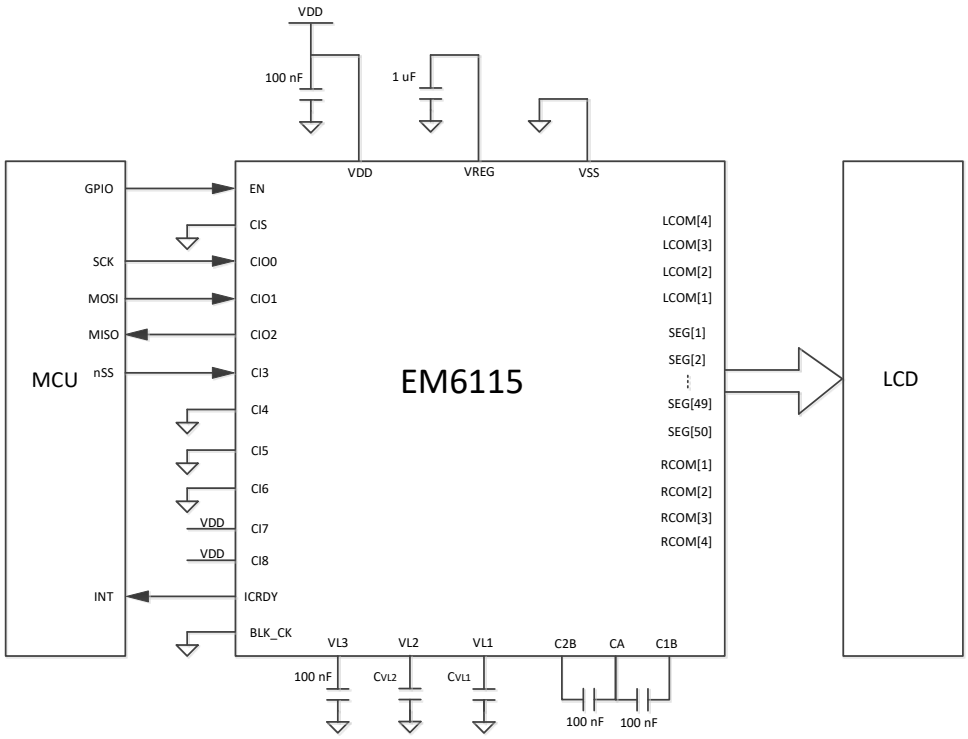



**Figure 4-1 : Bias ⅓ & Static 3 x $V_{REF}$ (see Note [19])**

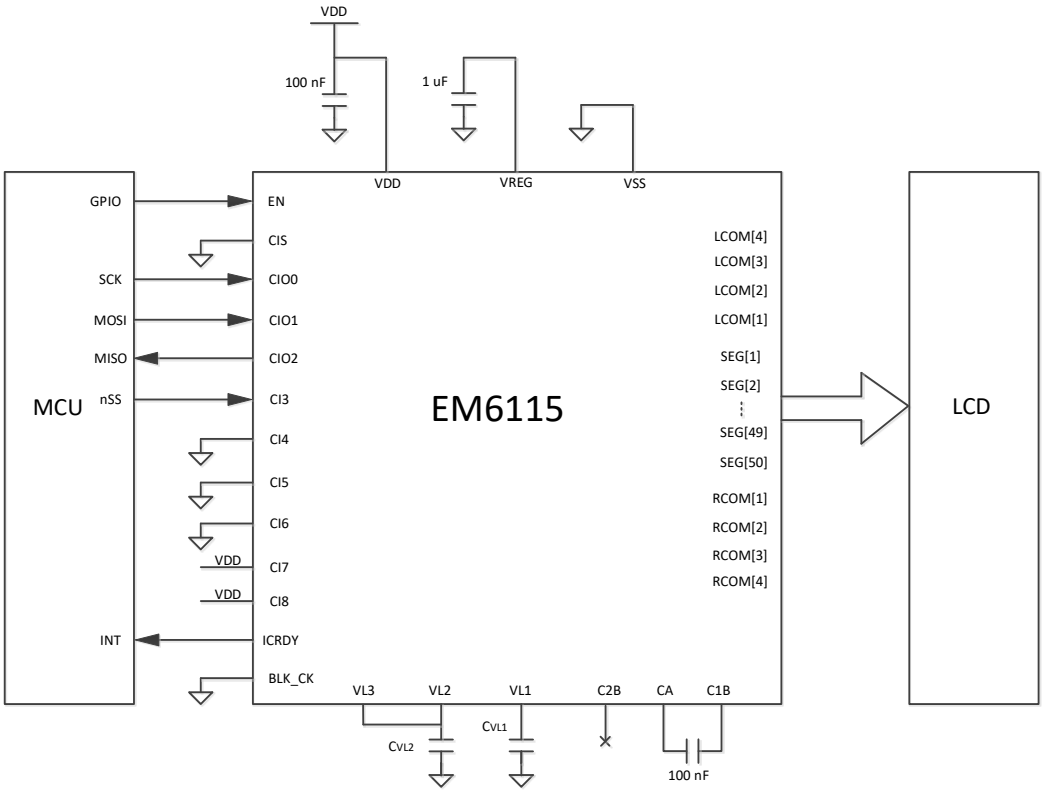



**Figure 4-2 : Bias ½, Static $V_{REF}$ / 2 & Static 2 x $V_{REF}$ (see Note [20])**

[19] For values of $C_{VL1}$ and $C_{VL2}$ see chapters 2.1.2 and 2.1.3
[20] For values of $C_{VL1}$ and $C_{VL2}$ see chapters 2.1.2 and 2.1.3

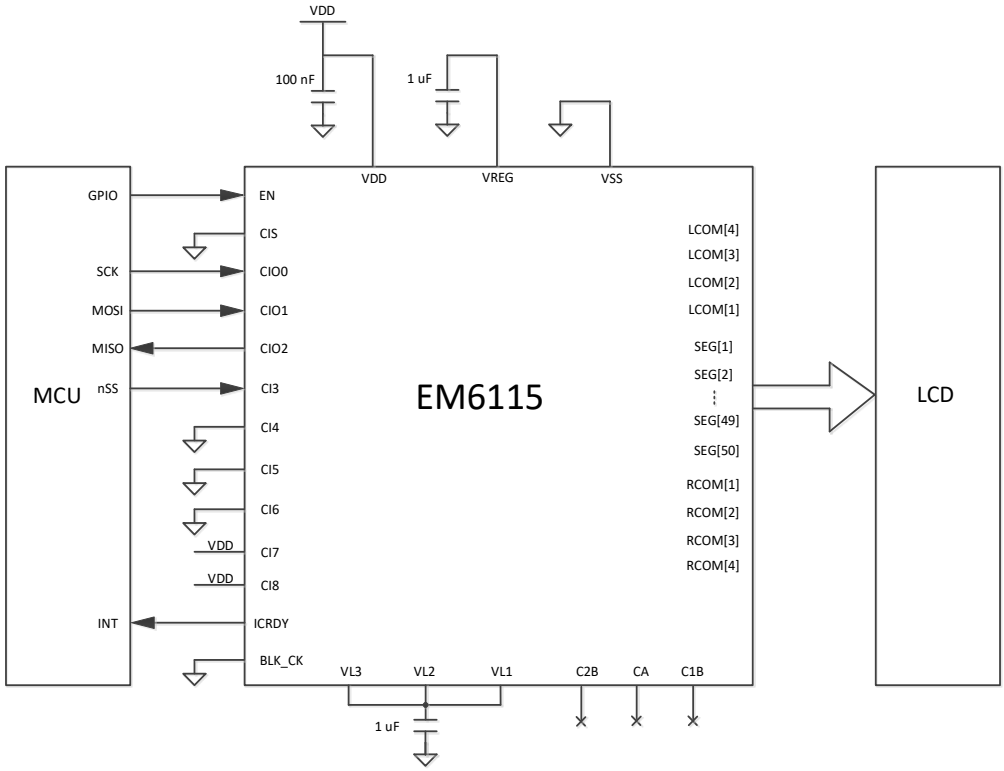



**Figure 4-3 : Static $V_{REF}$**

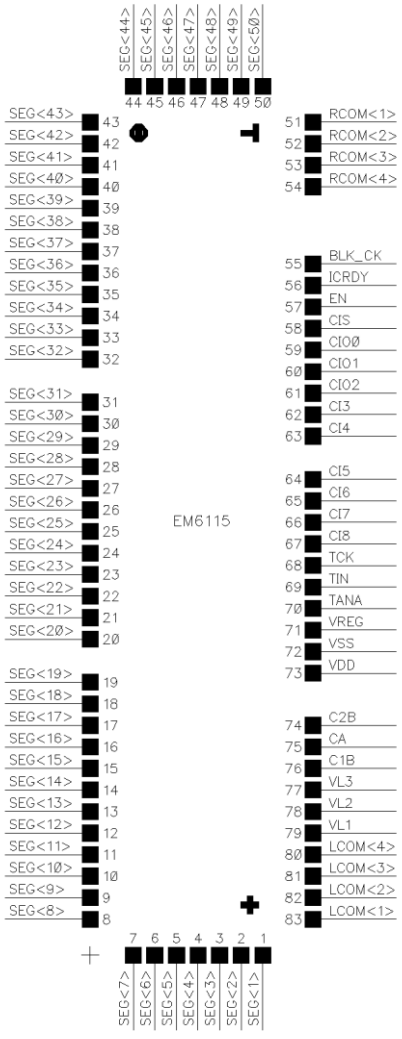
## 5. PAD LOCATION DIAGRAM

Pad location with a pitch of 90 µm
Pad opening:

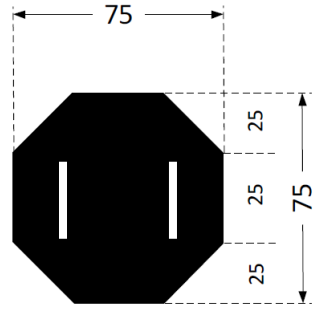
- Standard pad for wire bonding 68 x 68 µm$^2$ ; Material : Al-Cu 8000A
- Gold Bump on pad 74 x 74 µm$^2$ ; Material : Au
  Height 17.5 µm +/- 2 µm
  Hardness 57 Hv +/- 20 Hv

Chip Size: 3852 µm x 1152 µm = 4.438 mm$^2$
Either wire bonded or flip chip bonded
Substrate connected to VSS

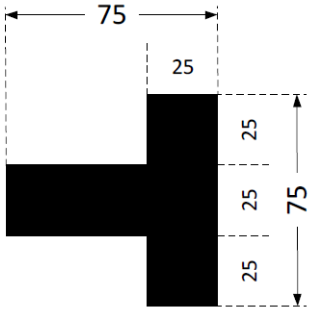
Chip assembly must protect the backside and the front side of the die from light. Effects of light may affect device reliability or cause malfunction.



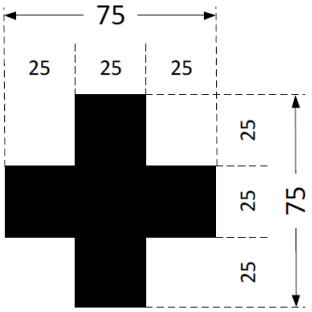

**Alignment marks:**




Octagon center: X = 273.71 µm; Y = 3505.53 µm




Letter T center: X = 737.35 µm; Y = 3505.53 µm




Cross center: X = 737.35 µm; Y = 280.385 µm

Notes: The origin (0,0) microns is the lower left coordinate of center pads.
Pad to scribe right: 76.78 µm
Pad to scribe left: 77.22 µm
Pad to scribe top: 77.09 µm

Pad to scribe bottom: 76.91 µm

## 5.1. PAD COORDINATES

| # | Pin name | X in µm | Y in µm | # | Pin name | X in µm | Y in µm |
|---|---|---|---|---|---|---|---|
| 1 | SEG<1> | 720 | 0 | 43 | SEG<43> | 0 | 3480 |
| 2 | SEG<2> | 630 | 0 | 44 | SEG<44> | 180 | 3630 |
| 3 | SEG<3> | 540 | 0 | 45 | SEG<45> | 270 | 3630 |
| 4 | SEG<4> | 450 | 0 | 46 | SEG<46> | 360 | 3630 |
| 5 | SEG<5> | 360 | 0 | 47 | SEG<47> | 450 | 3630 |
| 6 | SEG<6> | 270 | 0 | 48 | SEG<48> | 540 | 3630 |
| 7 | SEG<7> | 180 | 0 | 49 | SEG<49> | 630 | 3630 |
| 8 | SEG<8> | 0 | 150 | 50 | SEG<50> | 720 | 3630 |
| 9 | SEG<9> | 0 | 240 | 51 | RCOM<1> | 930 | 3480 |
| 10 | SEG<10> | 0 | 330 | 52 | RCOM<2> | 930 | 3390 |
| 11 | SEG<11> | 0 | 420 | 53 | RCOM<3> | 930 | 3300 |
| 12 | SEG<12> | 0 | 510 | 54 | RCOM<4> | 930 | 3210 |
| 13 | SEG<13> | 0 | 600 | 55 | BLK_CK | 930 | 2888 |
| 14 | SEG<14> | 0 | 690 | 56 | ICRDY | 930 | 2798 |
| 15 | SEG<15> | 0 | 780 | 57 | EN | 930 | 2708 |
| 16 | SEG<16> | 0 | 870 | 58 | CIS | 930 | 2618 |
| 17 | SEG<17> | 0 | 960 | 59 | CIO0 | 930 | 2528 |
| 18 | SEG<18> | 0 | 1050 | 60 | CIO1 | 930 | 2438 |
| 19 | SEG<19> | 0 | 1140 | 61 | CIO2 | 930 | 2348 |
| 20 | SEG<20> | 0 | 1320 | 62 | CI3 | 930 | 2258 |
| 21 | SEG<21> | 0 | 1410 | 63 | CI4 | 930 | 2168 |
| 22 | SEG<22> | 0 | 1500 | 64 | CI5 | 930 | 1988 |
| 23 | SEG<23> | 0 | 1590 | 65 | CI6 | 930 | 1898 |
| 24 | SEG<24> | 0 | 1680 | 66 | CI7 | 930 | 1808 |
| 25 | SEG<25> | 0 | 1770 | 67 | CI8 | 930 | 1718 |
| 26 | SEG<26> | 0 | 1860 | 68 | TCK | 930 | 1628 |
| 27 | SEG<27> | 0 | 1950 | 69 | TIN | 930 | 1538 |
| 28 | SEG<28> | 0 | 2040 | 70 | TANA | 930 | 1448 |
| 29 | SEG<29> | 0 | 2130 | 71 | VREG | 930 | 1358 |
| 30 | SEG<30> | 0 | 2220 | 72 | VSS | 930 | 1268 |
| 31 | SEG<31> | 0 | 2310 | 73 | VDD | 930 | 1178 |
| 32 | SEG<32> | 0 | 2490 | 74 | C2B | 930 | 960 |
| 33 | SEG<33> | 0 | 2580 | 75 | CA | 930 | 870 |
| 34 | SEG<34> | 0 | 2670 | 76 | C1B | 930 | 780 |
| 35 | SEG<35> | 0 | 2760 | 77 | VL3 | 930 | 690 |
| 36 | SEG<36> | 0 | 2850 | 78 | VL2 | 930 | 600 |
| 37 | SEG<37> | 0 | 2940 | 79 | VL1 | 930 | 510 |
| 38 | SEG<38> | 0 | 3030 | 80 | LCOM<4> | 930 | 420 |
| 39 | SEG<39> | 0 | 3120 | 81 | LCOM<3> | 930 | 330 |
| 40 | SEG<40> | 0 | 3210 | 82 | LCOM<2> | 930 | 240 |
| 41 | SEG<41> | 0 | 3300 | 83 | LCOM<1> | 930 | 150 |
| 42 | SEG<42> | 0 | 3390 | | | | |

**Table 27 : Pad coordinates for wire bond and Gold Bump finish**

# 6. PACKAGE INFORMATION

Please contact EM Microelectronic-Marin for available package options

## 7. CUSTOMER DELIVERY: DEFAULT CONFIGURATION

| Function | Addr | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| - | $00 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … |
| End_address | $09 | - | End_Addr [6:0] = $09 | | | | | | | - | - | - | - | - | - | - | - |
| N/A | $0A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … | … |
| N/A | $7F | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

**Table 28: EEPROM content delivered to customer**

The configuration registers and dictionary are not defined in the EEPROM delivered to customers, as the value of End_Addr is limited to the reserved area. Therefore, the default configuration of the circuit is given by the reset values of both configuration registers and dictionary:

- The reset values of configuration registers can be found in the section 2.7.2.
- The reset values of dictionary are all '0' and, therefore, all physical segments are mapped to the bit 0 of the group 0 (named A0) in the internal registers.

## 8. ORDERING INFORMATION

| Part Number | Delivery Form |
|---|---|
| EM6115V3WS8 | Standard pads, Sawn wafer on frame, 8 mils thickness |
| EM6115V3WS11E | Gold Bump , Sawn wafer on frame, 11 mils thickness |
| EM6115V3xxx | For other options, please contact the EM Microelectronic-Marin SA sales representative. |