3V Self Recovering Watchdog

Description

The H6061 is a combined initialiser, watchdog and voltage monitor. The circuit is a low voltage low power monolithic CMOS device combining a series of voltage comparators and a programmable timer on the same chip. The device is specially suited to telecommunications applications where 3 V working is expected, for functions such as supply voltage and microprocessor monitoring. The reset outputs are self recovering after a watchdog timeout, enabling the circuit to work with standalone systems without any external push-switch or control signal to restart after a watchdog timeout. The circuit provides a reset signal of both polarities. The state of the outputs is defined down to 1.6 V. An internal debouncer ensures power-up performance for fast-rise supply lines.

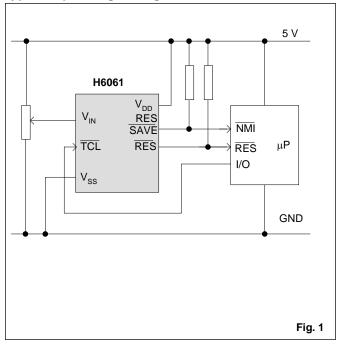
Features

- ☐ Watchdog fully operational from 2.7 to 5.25 V
- ☐ Regulated DC voltage monitor, internal voltage reference
- ☐ Self recovering watchdog function: reset goes active after the 1st timeout period, reset goes inactive again after the 2nd timeout period, repeated active reset signal until the system recovers
- ☐ Standard timeout period and power-on reset time (100 ms), externally programmable from 3 ms to 3 mins if required
- ☐ Works down to 1.6 V supply voltage
- ☐ Low voltage alarm prior to reset on power-down
- Reset outputs of both polarities
- Open drain outputs
- SO8 package

Applications

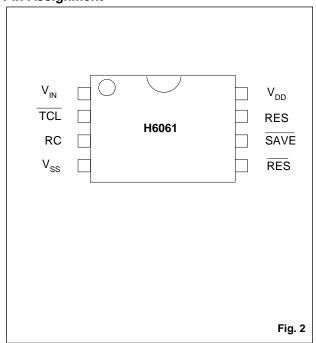
- Microprocessor and microcontroller systems
- Point of sales equipment
- ☐ Telecom products
- Automotive subsystems
- ☐ Microcontroller 68HC05 applications

Typical Operating Configuration



Pin Assignment

1





Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V _{DD} to V _{SS}	V_{DD}	– 0.3 to + 5.6 V
Voltage at any pin to Vss	V_{MIN}	- 0.3
Voltage at any pin to V _{DD}	V_{MAX}	+ 0.3
Voltage at V _{IN} to V _{SS}	VINMAX	+ 12 V
Current at any output	I _{MAX}	± 10 mA
Storage temperature	T _{STO}	-65°C to +150°C
Electrostatic discharge max. to MIL-STD-833C method 3014	V_{Smax}	1000V

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating temperature Industrial	T _{AI}	-40	+85	°C
Supply voltage	V_{DD}	2.7	5.25	V
Version 11,12	VIN	0	12	V
RC-oscillator programming				
External capacitance*	C1		1	μF
External resistance	R1	10		kΩ

^{*} Leakage < 1μA

Table 2

Electrical Characteristics

 V_{DD} = 5.0 V, T_A = -40 to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Units
V _{DD} activation threshold	V _{ON}	T _A = 25 °C	2.3		2.7	V
V _{DD} deactivation threshold	Voff	T _A = 25 °C		Von-0.3		V
Supply current	I _{DD}	RC open, TCL at V _{DD} or V _{SS}		80	140	μΑ
Input V _{IN} , TCL		1.10 spo, 1.02 at 188 at 188				
Leakage current	lР	V _{SS} < V _{IP} <v<sub>DD T_A = 80 °C</v<sub>		0.005	1	μΑ
TCL input low level	VIL				0.8	V
TCL input high level	ViH		2.4			V
Leakage on pins SAVE, RES, RES	lolk	$V_{OUT} = V_{DD}$		0.050	1	μΑ
O/P drive logic low	loL	$V_{OL} = 0.4 V$	4	8		mΑ
	loL	$V_{DD} = 3.5 \text{ V}; V_{OL} = 0.4 \text{ V}$	2			mA
	loL	$V_{DD} = 1.6 \text{ V}; V_{OL} = 0.4 \text{ V}$	80			μΑ

Table 3

VIN Surveillance

Voltage thresholds at T_A = 25 °C

Version No.	Thresho V _{SH} V _{SL}		at V _{DD}	Threshold Voltage Tolerance	Threshold Ratio*	Pin V _{IN} Input
25	1.54 1.50	1.46	2.7 – 5.0 V	±10%	±2%	~100 MΩ

^{*} Threshold ratio defined as V_{SH} / V_{SL} or V_{SL} / V_{RL}

Table 4

Timing Characteristics

 $V_{DD} = 5.0 \text{ V}$, $T_A = -40 \,^{\circ}\text{C}$ to $+85 \,^{\circ}\text{C}$, unless otherwise specified

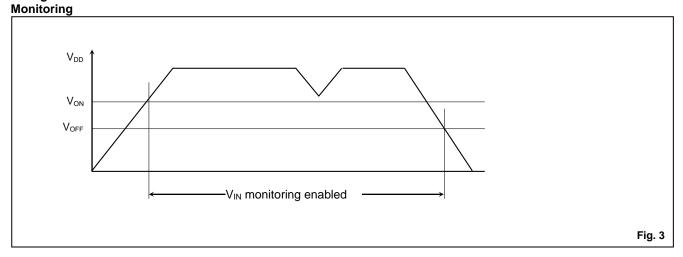
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Units
Propagation delays						
TCL to output pins	T _{DIDO}			250	500	ns
V _{IN} to output pins	TAIDO	Excluding debounce time T _{DB}		4	10	μS
Logic transition times on all output pins	T _{TR}	Load 10 kΩ, 100 pF		30	100	ns
Timeout period	T _{TO}	RC open, unshielded, T _A = 25 °C	60	100	160	ms
T _{TCL} input pulse width	T _{TCL}		150			ns
Power-on reset debounce	T _{DB}			T _{TO} /64		ms
Fastest pulse V _{IN} with debounce	T_{VINL}	-40 to +85 °C	10			μS

2

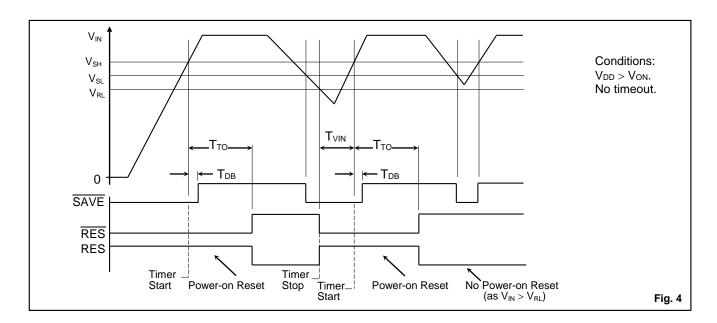
Table 5



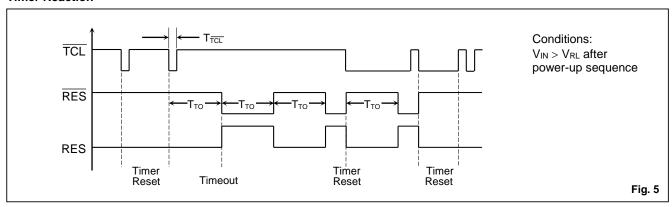
Timing Waveforms Voltage Reaction: VDD



Voltage Reaction: V_{IN} Monitoring

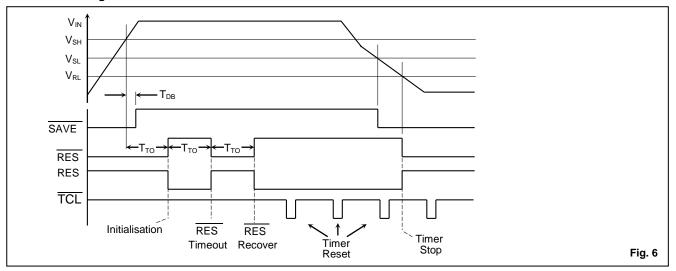


Timer Reaction

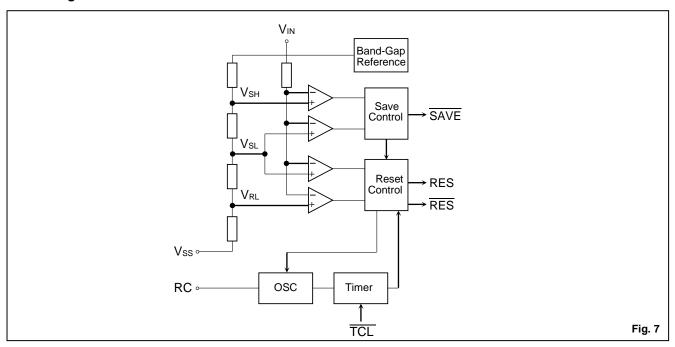




Combined Voltage and Timer Reaction



Block Diagram





Pin Description

Pin	Name	Function
1	VIN	Voltage monitoring input
2	TCL	Timer clear input signal
3	RC	RC oscillator tuning input
4	V_{SS}	GND terminal
5	RES	Reset output, open drain
6	SAVE	Save output, open drain
7	RES	Positive reset output, open drain
8	V_{DD}	Positive supply voltage

Table 6

Functional Description

Thresholds and Outputs

The H6061 has open-drain outputs and voltage thresholds on pin V_{IN} of typically 1.5 V.

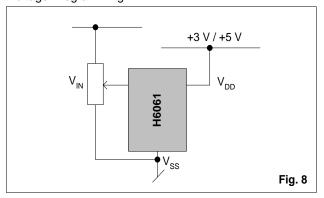
Internal Voltage Comparators

The voltage comparators detect the voltage applied to pin V_{IN} and compare it with thresholds $V_{\text{SH}}, \ V_{\text{SL}}$ and $V_{\text{RL}}.$ The H6061 is designed for monitoring regulated DC voltages and has bandgap thresholds independent of V_{DD}. The reaction of the H6061 to voltage changes on pin V_{IN} is given in Fig. 4. During powering-up, the outputs are active. After VIN reaches the VSH level, pin SAVE deactivates after a short debounce time TDB to allow for fast ramp-ups. The initialization time T_{TO} then passes before the two reset outputs go inactive. Thereafter, when the voltage on pin V_{IN} falls below the V_{SL} level, pin SAVE goes active low as a first warning. If V_{IN} then drops below the V_{RL} level, the reset signals go active and are guaranteed down to 1.6 V. The reset outputs react also to timeouts (see "Timer clearing"). Note that when the supply voltage V_{DD} is below the level Voff (about 2.2 V), all outputs are in the active state for any allowed voltage of V_{IN}.

Voltage Programming

The H6061 was designed to give the best compromise in normal usage (see Table 3). Its voltage threshold can be programmed by an external resistor divider or a potentiometer to react at proportionally higher voltage levels (see Fig. 8 below).

Voltage Programming



Timer Programming

A single timeout period T_{TO} is used for the initialization reset duration and the watchdog timeout. With pin RC unconnected, the on-chip RC oscillator and divider chain give a timeout period T_{TO} of typically 100 ms. A resistor to V_{DD} will shorten this time, and a capacitor to V_{SS} will lengthen it (see Fig. 11). An approximation for calculating trial values given in milliseconds by the formula:

$$T_{TO} = \begin{bmatrix} 0.75 + \frac{(32 + C_1) \cdot 1.6}{V_{DD} - 0.8} \\ 4.8 + \frac{V_{DD} - 0.8}{R_1} \end{bmatrix} \cdot 8.192$$

 $R_{1~\text{min.}}$ = 10 k $\Omega,~C_{1~\text{max.}}$ = 1 μF If R_{1} is in $M\Omega$ and C_{1} in pF, T_{TO} will be in ms.

Choice of component values must be determined in practice. To have a square wave of period $2T_{TO}$, simply connect pin \overline{TCL} to V_{DD} or V_{SS} and take the signal output from a reset pin.

Timer Clearing

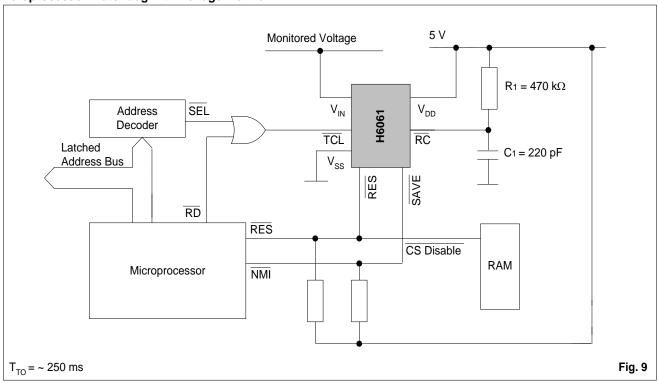
A negative edge or pulse at the \overline{TCL} input longer than 150 ns will clear the timer and deactivate the reset outputs under normal running conditions (see Fig. 3). \overline{TCL} will however have no effect either when $V_{DD} < V_{OFF}$ or during the initialization period before the deactivation of the reset pins.

Combined Voltage and Timer Action

In Fig. 6 is a typical sequence of power-up, watchdog run, and power-down. During initialization the SAVE pin deactivates one debounce delay time T_{DB} after V_{IN} rises above V_{SH} , or when the power line V_{DD} rises above V_{ON} , whichever happens last. The reset pins only deactivate one timeout period T_{TO} afterwards to free the watchdog timer and end the initialization. Note that either V_{IN} falling below V_{RL} threshold or V_{DD} below V_{ON} will cause an initialization upon recovery. Following initialization, the watchdog timer will time out after time T_{TO} unless at least one TCL pulse clears it. On timeout the reset pins reactivate for a further T_{TO} period before deactivating again for another try. A \overline{TCL} pulse will deactivate any timeout reset, and another TCL pulse must follow within a time T_{TO} to keep reset inactive. If no TCL pulses come at all, the reset pins go square-wave. Power-down overrides all this however. A falling voltage on V_{IN} gives a warning $\overline{SAVE} = 0$ signal at $V_{IN} = V_{SL}$ before activating the reset pins as soon as V_{IN} drops below V_{RL}. The H6061 has fixed thresholds and low hysteresis for monitoring regulated DC lines. Additional protection is provided in case V_{DD} supply falls over about 10% below V_{ON} which thereupon activates all outputs at once.



Typical Applications Microprocessor Watchdog with Voltage Monitor



Selection of Watchdogs for Each Application

The H6061 is designed for monitoring regulated DC voltages anywhere between 2.7 and 5.25 V. Typically, it is used to monitor V_{DD} with pin V_{IN} tied to the midpoint of a voltage divider (see Fig. 8). This arrangement has the advantage of being able to trigger at selectable voltage limits, i. e. it can be used where the regulated voltage is below 5 VDC.

Industrial Heavy-Duty Utilisation

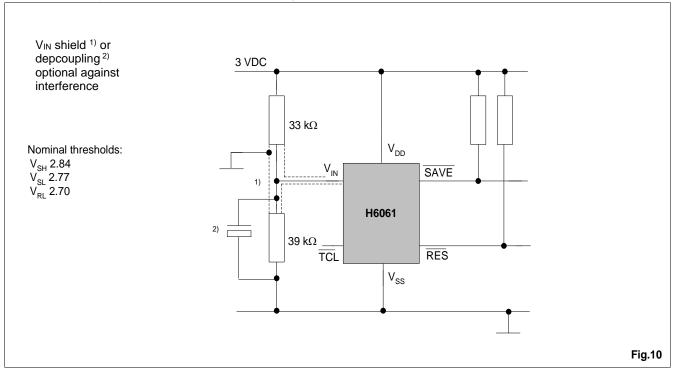
The H6061 debounce protects against reactions due to fast-rise power lines, but absolute maximum ratings must be respected. With its flexibility of voltage programming and supply voltage the H6061 can allow for voltage drops along supply lines, so it can be placed remotely, like on plug-in boards (see Fig. 9). The H6061 is suitable for supply voltages down to 2.7 VDC. As the H6061 is designed to be sensitive to voltage changes, fast switching lines, like address/data bus lines should not be run between the $V_{\rm DD}$ and $V_{\rm SS}$ supply lines near the H6061 without ground-plane shielding. Tracks from components to pin RC must be kept very short. Pin RC if left free should be shielded with a ground ring in noisy environments.

The H6061 has only 40 mV hysteresis specially for monitoring regulated DC. Pin V_{IN} must be protected from any significant mains ripple or RFI (see Fig. 10). It should be placed as near as possible to the point where voltage is to be monitored. Pin V_{IN} is protected by an internal resistor (nominal 15 k Ω) against voltages in excess of V_{DD} . In some environments this may however pick up enough mains ripple or RFI to distort the voltage detection thresholds or even cause unwanted sporadic resets in the absence of adequate shielding or filtering on V_{IN} .

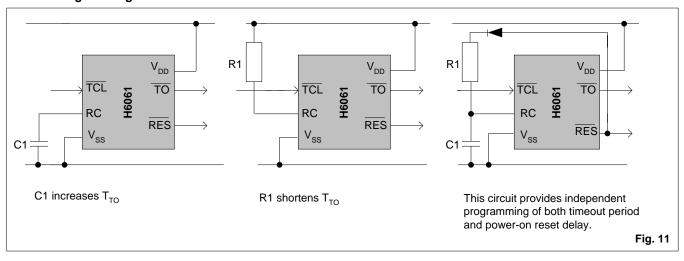
The H6061 has sufficient immunity to ripple and interference on the V_{DD} supply line, but if it is important that a system meet severe criteria for injected spikes and RFI, then care must be taken also decouple V_{DD} from these influences, as system protection must continue even under these conditions. With normal series voltage regulators, the regulated 5 VDC output voltage follows the DC rough voltage within 1.5 V on powering up. If the application has pin V_{IN} monitoring the DC rough, the internal inputs to the on-chip comparators will not rise above V_{DD} if the H6061 is correctly programmed. With switched-mode power supplies however, the DC-rough voltage on power-up rises almost to its working level before the 5 VDC line starts to ramp up. The H6061 has been specially designed to work under these extreme conditions but care must be taken not to exceed absolute maximum ratings. In addition to the voltage monitoring on pin V_{IN}, a final protection is given by the H6061 monitoring its own V_{DD} supply. If a system malfunction causes V_{DD} to fall below V_{OFF} even though pin V_{IN} stays high, then all outputs go active at once.



Combined Supply Monitor, Initializer and Watchdog

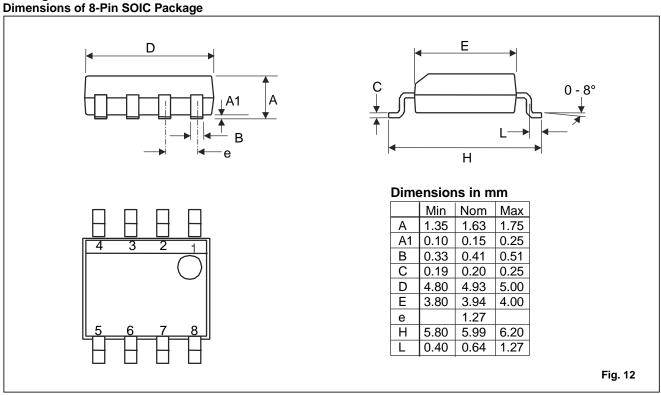


External Programming of RC Oscillator





Package Information



Ordering Information

When ordering, please specify the complete Part Number

Part Number	Version	Package	Delivery Form	Package Marking (first line)	Temperature
H6061V25SO8A	V2E	8-pin SOIC	Stick	606125	40°C to 195°C
H6061V25SO8B	V25	8-pin SOIC	Tape&Reel	606125	-40°C to +85°C

Note: other versions are no longer available

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