EM8500 FAQ

POWER MANAGEMENT CONTROLLER WITH ENERGY HARVESTING INTERFACE

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1. REGISTERS AND EEPROM

Q **How does a user configure EM8500 (MPPT ratio, supervising levels, supervising frequencies)? Is a resistor bridge used?**

A No. An internal EEPROM is used to store the settings – the default values are read during the **EM8500** boot phase, before the **VSUP**, and optionally some **VAUX**, is/are enabled.

Q **How does one communicate with the EM8500?**

A There is a SPI and an I²C interface. The default interface is I²C. By driving **CS** (Chip Select line) to '1' the SPI interface is selected and remains enabled until the **EM8500** is powered off. To use the I²C interface, CS (Chip Select line) must be tied to '0'.

Q **Which SPI modes are supported?**

A The EM8500 SPI supports two of the Motorola modes

- CPOL=1 and CPHA=1
- CPOL=0 and CPHA=0

The mode is automatically detected and selected. It is determined by the SCL value after the **CS** (Chip Select line) rising edge.

Q **Is the EEPROM usable by the end-user?**

A Yes. Read and write access to the EEPROM user area is possible. However, as no protection against a power drop or a power loss is present (anti-tearing) sufficient energy must be maintained during EEPROM access to safely complete a write operation.

Q **Is EEPROM multi-read access supported?**

A No. The internal timing of the EEPROM doesn't allow the use of multi-read access.

Q **Why are some registers non-writable?**

A Some registers are protected against spurious write access. It is necessary to unlock the access by writing first the key **0x4B** to register **reg_protect_key** in the same write transaction – for SPI communication I²C by keeping **CS** (Chip Select line) to ‘1’ or for I²C by completing accesses before the I²C stop condition occurs.

The protected registers are located in the address range **0x00** to **0x18**.

Q **Why can the EEPROM not be written?**

A The EEPROM area is protected against spurious write access (with the exception of the user area). As for the protected registers, it is necessary to unlock the access by writing first the key **0xA5** to register **reg_protect_key** in the same write transaction I²C – for SPI communication by keeping **CS** (Chip Select line) to ‘1’ or for I²C by completing accesses before the I²C stop condition occurs.

Q **Why does writing 0xAB into reg_soft_res_word have no effect?**

A This register is protected against spurious write. Starting by writing first the key **0xE2** to register **reg_protect_key** unlocks the register **reg_soft_res_word**. Both registers must be written in the same transaction I²C – for SPI communication by keeping **CS** (Chip Select line) to ‘1’ or for I²C by completing accesses before the I²C stop condition occurs.

2. HARVESTER

Refer to application note: e8500_app_note_hrv_param.pdf

Q **Is a quick start-up possible with energy available only from the harvester?**

A Yes. The dual storage architecture allows starting-up quickly powered only by the harvester. There is no need to wait for the battery charging process to supply the application.

Q **What are the possible MPPT ratios?**

A The user is able to select from 13 values: 50% especially for TEG and 60%, 67%,71%, 75%, 78%, 80% 82%, 83%, 85%, 86%, 87%, 88% especially for solar cells (typically about 80%).

Q **The EM8500 includes a lux-meter. How is it calibrated with respect to a solar-cell?**

A The lux-meter function is based on a short-cut current level detector: It has 16 levels. Levels have a logarithmic progression from 1µA to 32.768mA. The equivalent illuminance in lux is given by the characteristics of the solar cell.

Q **What is the recommended coil value?**

A 47µH

Q **Why not using a lower coil value such as 22µH?**

A This is a trade-off at low input power between good efficiency and the minimum coil value. Indeed, when operating at low input power, the intrinsic consumption of the oscillator needed for the DCDC is critical. Having a lower value coil requires a higher frequency.

Q **What is the battery consumption of EM8500 when the harvester is not providing any current?**

A In “HRV low” mode – i.e. when the harvester is too weak – the **EM8500** current consumption is typically 145nA. When the battery is in protected mode, the consumption is typically 65nA.

Q **Is the DCDC always enabled, even when the harvester is not providing energy?**

A No. The harvester is internally controlled to switch off the DCDC when not needed. The user can also force the DCDC off.

Q **The input voltage is limited to 1.8V on the harvester side. Does the EM8500 allow operation at 3V or 5V?**

A No. The device is designed to be used with a single or dual solar cell or TEG with low input power. Voltage levels above 1.8V are not generated by such harvesters.

Q **Is there a protection should the voltage on the harvester side exceed 1.8V?**

A No. There is no overvoltage protection. EM8500 is targeting input voltages up to 1.8V.

Q **Is the EM8500 able to handle negative voltages on the harvester input?**

A No. The **EM8500** is designed for positive DC harvester input voltages only. It is possible to use an external rectifier, but this has an impact on the minimum harvested input voltage/consumption and, consequently, on efficiency.

3. STORAGE ELEMENTS

Refer to application note: e8500_app_note_store_supervise.pdf

Q **Is it possible to use EM8500 to extend the life time of a primary cell battery?**

A Yes. An EEPROM configuration is available to cover this use case. In such mode the **EM8500** supplies the application from the harvester as long as possible. If this harvester energy is too low, the **EM8500** supplies the application using energy from the battery.

Q **Is the battery protected against over voltage?**

A Yes. When the battery reaches its maximum voltage level, the DCDC is automatically stopped. This level is configurable in EEPROM.

Q **Is the battery protected against under voltage?**

A Yes. When the battery drops to its minimum voltage level, the EM8500 enters in “battery protection” mode. The battery is disconnected and stops supplying the application. Only the energy from the harvester supplies the application in this mode.

Q **What is the purpose of v_bat_min_lo and v_bat_min_hi?**

A These two levels are the minimum voltages of the battery and the application. Below this level the **EM8500** enters into “battery protection” mode. These two voltage levels form a hysteresis. Both are configurable independently in the EEPROM.

Q **What is the difference between v_bat_min_hi_con and v_bat_min_hi_dis?**

A One is used when STS and LTS are disconnected **(v_bat_min_hi_dis**), the other when STS and LTS are connected (**v_bat_min_hi_con**). When STS and LTS are disconnected the hysteresis shall be larger because STS drops quickly compared to LTS when there are unconnected in case there is no energy available from the harvester.

Q **What is the purpose of v_apl_max_lo and v_apl_max_hi?**

A They define the maximum application voltage. These two levels form a hysteresis. When STS rises above this level, the LDO supplying **VSUP** is automatically enabled to limit the application voltage supply level.

Q **What is the purpose of v_bat_max_hi and v_bat_max_lo?**

A They define the maximum battery voltage. These two levels form a hysteresis. When LTS and STS rise above **v_bat_max_hi**, the DCDC stops charging the battery, when they fall below **v_bat_max_lo**, the DCDC restart charging the battery.

Q **What are the supervising frequencies of STS and LTS storage elements?**

A It depends on what element is supervised and when

STS:

- Harvester DCDC enabled,
  STS and LTS disconnected from each other: between 1kHz and 4Hz
- Harvester DCDC enabled,
  STS and LTS connected to each other: between 8Hz and $^{1}/_{16}$Hz
- Harvester DCDC off,
  STS and LTS connected to each other: between 500Hz and $^{1}/_{32}$Hz

LTS (when STS and LTS are connected only STS is supervised):

- Harvester DCDC enabled : between 8Hz and $^{1}/_{16}$Hz
- Harvester DCDC off : between 500Hz and $^{1}/_{32}$Hz

4. OUTPUT SUPPLIES

Refer to application note: e8500_app_note_supply_control.pdf

Q **Is it possible to supply an application only with the energy from the harvester, without a battery connected to EM8500?**

A yes. For this mode the **EM8500** has to be configured in primary cell mode in EEPROM. LTS is connected to the ground.

Q **What is the trigger level of the wake-up pin?**

A Wake-up is triggered to '1' above 0.9V (typ.) and to '0' below 0.5V (typ.). Its voltage reaches the level of the highest voltage connected to the device.

Q **Can the internal wake-up counter be disabled?**

A No. This timer ensures that the application cannot switch itself off without having any means of recovery.

Q **What is the timer accuracy?**

A The timer clock source is not trimmed and therefore not highly accurate. The oscillator is primarily designed for low-power operation. However, it is possible to trim the counter value with the help of an accurate timing source.

Q **How long does it take to wake-up my CPU when the interrupt (wake-up pin) is asserted?**

A It depends on the configuration but in the main cases (no de-bouncing circuit, with a rising event) it typically requires 2.2ms between the event and the switch on of the **VSUP** output.

Q **Why is a supervisory level configured through the wizard not identical to one I configured?**

A The wizard uses the MIN/MAX LSB value of the VLD (Voltage Level Detector) to ensure the different voltages never cross the levels set by the user in any conditions. The levels used in the timing diagram are based on TYPICAL LSB value of the VLD.