Application Note 608003

Title: **STORAGE ELEMENTS STS/LTS SUPERVISING**

Product Family: **EM850X**

Part Number: EM8500

Keywords: Harvesting, Solar, TEG, MPPT, Configuration, Setup, Super capacitors, Secondary Battery, Primary Battery

ABSTRACT

The EM8500 offers a NVM containing all the configuration parameters. This document describes how to setup the registers in NVM linked to the storage elements connected to STS & LTS:

- Type of battery: rechargeable (secondary battery) or non-rechargeable (primary battery)
- Under voltage protection enabled or disabled
- Voltage level detection:
  - maximum/minimum battery level settings
  - maximum application voltage
- Voltage measurement timing settings

ABBREVIATIONS

NVM	Non-Volatile-Memory
MCU	Microcontroller Unit
STS	Short term storage element (capacitor connected to VDD_STS)
LTS	Long term storage element (rechargeable battery connected to VDD_LTS)
HRV	Harvester, main source of energy (solar or TEG)
TEG	Thermal Electrical Generator
MPP	(Maximum Power Point) This operating point is reached when the harvester delivers the maximum power (Pmpp) in a given condition
Vmpp	HRV output voltage at MPP
Vov	HRV open voltage (when the EM8500 DCDC converter is disabled)
BAT_LOW	Flag indicating that the battery is in under-voltage condition
HRV_LOW	Flag indicating that the HRV is under the minimum power level (HRV low mode when at 1)
VLD	Voltage Level Detector
Vref	Voltage level detector reference level
Vlvl	Voltage level detector LSB (71.88mV)
Vbat	Battery voltage connected to VDD_LTS
VSUP	Main output supply for application
VAUX[i]	2 independent auxiliary supplies for application
Csup	Decoupling capacitor on VSUP
Caux[i]	3 decoupling capacitors on VAUX[i]

1 SCOPE

The EM8500 addresses two main types of mass storage elements connected to LTS:

1. Rechargeable
    a. secondary battery
    b. or super capacitor
2. Non-rechargeable for battery life time enhancement (so called primary cell mode)
    a. primary battery

On STS side, a standard capacitor in the range of 10uF to few 100uF is connected.
The EM8500 has several registers to setup the storage elements supervising:

1. Type of LTS used
2. Under and over voltage protection level of LTS settings
3. Regulation voltage level of STS when disconnected from LTS
4. Period of voltages measurement settings

The following registers are involved for that action:

Register name	Address	Description
reg_lts_cfg	0x06	*prim_cell_connect*: force the connection of STS to LTS in primary cell mode when at '1' *prim_cell*: set the device in primary cell mode when '1' *no_bat_protect*: under voltage protection disabled when at '1'
reg_v_bat_max_hi	0x07	Absolute maximum voltage level of the battery
reg_v_bat_max_lo	0x08	Maximum voltage of the battery, form an hysteresis with **v_bat_max_hi**
reg_v_bat_min_hi_dis	0x09	Minimum battery and application voltage when STS and LTS are disconnected, form an hysteresis with **v_bat_min_lo**
reg_v_bat_min_hi_con	0x0A	Minimum battery and application voltage when STS and LTS are connected, form an hysteresis with **v_bat_min_lo**
reg_v_bat_min_lo	0x0B	Absolute minimum value of the battery and the application
reg_v_apl_max_hi	0x0C	Absolute maximum voltage of the application
reg_v_apl_max_lo	0x0D	Maximum voltage of the application, form an hysteresis with **v_apl_max_hi**
reg_t_sts_period	0x02	Period between two voltage level measurements of STS, used only when STS and LTS are disconnected
reg_t_lts_period	0x03	Period between two voltage level measurements of LTS
reg_t_hrv_low_cfg	0x17	*t_lts_hrv_low_period*: Define the period between two voltage level measurements of LTS in HRV low mode

Table 1: List of Registers Related to Storage Elements Supervising

The default value after reset or start-up of the registers listed in Table 1 is contained in a NVM memory at the following related addresses:

Register name	Register Address	Related address in NVM	
reg_lts_cfg	0x06	eeprom6	0x46
reg_v_bat_max_hi	0x07	eeprom7	0x47
reg_v_bat_max_lo	0x08	eeprom8	0x48
reg_v_bat_min_hi_dis	0x09	eeprom9	0x49
reg_v_bat_min_hi_con	0x0A	eeprom10	0x4A
reg_v_bat_min_lo	0x0B	eeprom11	0x4B
reg_v_apl_max_hi	0x0C	eeprom12	0x4C
reg_v_apl_max_lo	0x0D	eeprom13	0x4D
reg_t_sts_period	0x02	eeprom2	0x42
reg_t_lts_period	0x03	eeprom3	0x43
reg_t_hrv_low_cfg	0x17	eeprom23	0x57

Table 2: Mapping of Registers in EEPROM

Note: offset between the register addresses and related address in NVM is 0x40

2 SUPERVISING REGISTERS SETTINGS SEQUENCE

We advise calculating the different parameters in the following order:

1. Chapter 4: The operating mode: rechargeable battery, primary cell mode, battery protection (*reg_lts_cfg*)
2. Chapter 5: The absolute min/max voltages (*reg_v_bat_max_hi*, *reg_v_apl_max_hi*, *reg_v_bat_min_lo*)
3. Chapter 6: The capacitor value connected on VDD_STS (Csts).
4. Chapter 7: The VDD_STS supervisory period Tsts_period (*reg_t_sts_period*)
5. Chapter 0: The v_bat_min hysteresis (*reg_v_bat_min_hi_dis*, *reg_v_bat_min_hi_con*)
6. Chapter 9: The value of **v_apl_max_lo** (*reg_v_apl_max_lo*)
7. Chapter 10: The value of **v_bat_max_lo** (*reg_v_bat_max_lo*)
8. Chapter 11: The VDD_LTS supervisory period **Tlts_period** and Tlts_hrv_low_period (*reg_t_lts_period*, *reg_t_hrv_low_cfg*)

3 VLD REFERENCE

The VLD is used to compare the current state of the voltages VDD_STS or VDD_LTS with a selected reference. The following registers select the references related to a voltage level:

- *reg_v_bat_max_hi*: reference **v_bat_max_hi**
- *reg_v_bat_max_lo*: reference **v_bat_max_hi**
- *reg_v_bat_min_hi_dis*: reference **v_bat_min_hi** when VDD_STS & VDD_LTS are disconnected
- *reg_v_bat_min_hi_con*: reference **v_bat_min_hi** when VDD_STS & VDD_LTS are connected
- *reg_v_bat_min_lo*: reference **v_bat_min_lo**
- *reg_v_apl_max_hi*: reference **v_apl_max_hi**
- *reg_v_apl_max_lo*: reference **v_apl_max_lo**

These registers set the related reference level as follows:

$$V_{ref} = V_{lvl} \cdot (reg + 1)$$

Equation 1: VLD Reference Calculation

The precision of Vlvl is as follows:

	MIN(1)	**TYP**	**MAX(1)**
Vlvl	69 mV	73 mV	76.2 mV

Table 3: Vlvl Precision

(1) These values are based on a typical spread of voltage level detector.
If the reference level is the maximum value of the hysteresis (_hi), the maximum value of Vlvl is used to calculate the related register.
If the reference level is the minimum value of the hysteresis (_lo), the minimum value of Vlvl is used to calculate the related register.

4 OPERATING MODE SETTINGS

4.1 Battery type

The first step is to set the type of battery used:

- Rechargeable (secondary cell battery; *reg_lts_cfg.prim_cell* = '0')
- Non-rechargeable (primary cell battery; *reg_lts_cfg.prim_cell* = '1')

4.2 Battery protection

By default the EM8500 checks the under voltage condition of the battery. It is possible to disable this function by setting the register *reg_lts_cfg.no_bat_protect* to '1'. In this condition, the EM8500 will try indefinitely to start-up on the battery voltage. If there is no energy from the HRV, the EM8500 will start-up by connecting VDD_LTS to VDD_STS, execute the boot sequence, as VDD_LTS is lower than **v_bat_min_lo** it will disconnect VDD_STS and VDD_LTS, then VDD_STS will collapse and enter in power on reset. Therefore, the EM8500 will start-up again and loop in this sequence until energy is back from the HRV.
Note: We advise to avoid setting *reg_lts_cfg.no_bat_protect* to '1' with a rechargeable battery; it can damage the battery. It is preferable to do it only with a super capacitor.

4.3 Force connection of LTS to STS in primary cell mode

The register *reg_lts_cfg.prim_cell_connect* forces the connection of LTS to STS in primary cell mode (*reg_lts_cfg.prim_cell* = '1'). If this bit is set to '1' in the NVM (address 0x46), the connection will be effective after the start-up sequence. This bit has no effect when *reg_lts_cfg.prim_cell* = '0' or if VDD_LTS is lower than **v_bat_min_lo**.

5 ABSOLUTE VALUES SETTINGS

There are 3 absolute values to set up in the EM8500:

1. The maximum battery voltage: **v_bat_max_hi**
2. The maximum application voltage: **v_apl_max_hi**
3. The minimum battery voltage (considered also as minimum application voltage): **v_bat_min_lo**

5.1 Maximum battery voltage

This is the absolute overvoltage limit of the battery. When the supply VDD_LTS reaches this voltage, the EM8500 stops charging the battery. The register *reg_v_bat_max_hi* defines the absolute maximum battery voltage and is calculated as follows:

$$reg\_v\_bat\_max\_hi = \text{trunc}\left(\frac{v\_bat\_max\_hi}{\max(V_{lvl})} - 1\right) + 1$$

Equation 2: *reg_v_bat_max_hi* Calculation

5.2 Maximum application voltage

This level is used when the maximum battery voltage is higher than the voltage the application can afford. If VDD_STS is higher than this level, the EM8500 will automatically enable the LDO connected on VSUP to protect the application against overvoltage. The register *reg_v_apl_max_hi* defines the absolute maximum application voltage and is calculated as follows:

$$reg\_v\_apl\_max\_hi = \text{trunc}\left(\frac{v\_apl\_max\_hi}{\max(V_{lvl})} - 1\right) + 1$$

Equation 3: *reg_v_apl_max_hi* Calculation

If the application maximum voltage is higher than the maximum battery voltage, *reg_v_apl_max_hi* shall be set to 0x3F and *reg_v_apl_max_lo* shall be set to 0x3E. In this condition these two registers will be ignored.

5.3 Minimum battery voltage

The absolute under voltage condition level of the battery is **v_bat_min_lo**. When VDD_LTS is below that level, the battery is in protected mode and the flag BAT_LOW stays at '1' until VSUP is on. In that condition it is impossible to use the battery as source of energy, only the harvester can supply the application. The register *reg_v_bat_min_lo* defines this level as follows:

$$reg\_v\_bat\_min\_lo = \text{trunc}\left(\frac{v\_bat\_min\_lo}{\min(V_{lvl})} - 1\right)$$

Equation 4: *reg_v_bat_min_lo* Calculation

6 SHORT TERM STORAGE CAPACITOR SETTING

If the application is supposed to always run on LTS (VDD_STS always connected to VDD_LTS), we advise to use Csts= 10uF. But if STS supplies the application without the help of the battery or super capacitor, as it is the case in primary cell mode, the value of Csts shall be carefully calculated.
When VAUX[i] or VSUP is enabled, the decoupling capacitors Caux[i] or Csup is suddenly connected to Csts. Therefore the transfer of charges from Csts to the decoupling capacitor leads to a drop on VDD_STS. We advise to avoid a drop higher than 10% of VDD_STS.
Thus, Csts shall be 10 times bigger than the total amount of decoupling capacitors enabled in the same time.
For instance if VSUP and all VAUX[i] are enabled in the same time:

$$C_{STS} = 10 \cdot \left(C_{SUP} + C_{AUX[0]} + C_{AUX[1]} + C_{AUX[2]} \right)$$

Equation 5: Csts Calculaton; all Decoupling Capacitors Enabled Together

7 STS SURVEY PERIOD

The survey period affects the power loss of the VLD during the measurement of STS. Longer this period, lower the power loss. The register *reg_t_sts_period* is a number of t_frame of 1ms and is calculated as follows:

$$T_{sts\_period} = \frac{P_{vld} \cdot t\_frame}{4 \cdot P_{in\_min} \cdot VLD_{loss}} = \frac{3 \cdot 10^{-9}}{4 \cdot P_{in\_min} \cdot VLD_{loss}}$$

Equation 6: STS Survey Period Calculation

The parameter Pvld (in [W]) is the power dissipated by the VLD when enabled: 3uW (constant)
The parameter t_frame (in [s]) is the minimum period between 2 measurements: 1ms (constant)
The parameter Pin_min (in [W]) is the minimum power the EM8500 can harvest before entering in HRV_LOW mode.
The parameter VLDloss (without unit) is the rate of power the user accepts to lose in the VLD measurement of VDD_STS.
Important note: when VDD_STS is connected to VDD_LTS Tsts_period is not used anymore. The supervisory period is set by **Tlts_period** instead (see chapter 11). Therefore, there is no VLDloss due to STS measurement in that condition.
The register *reg_t_sts_period* shall be selected according to the following table to be the closest to Tsts_period:

reg_t_sts_period	**Tsts_period**
000	1ms
001	2ms
010	8ms
011	16ms
100	32ms
101	64ms
110	128ms
111	256ms

Table 4: Tsts_period Related Registers Selection

7.1 Example of STS survey period calculation

Considering that the EM8500 has been configured to stop harvesting energy when the input power is below 2uW:
Pin_min = 2uW
We accept to lose 1% of power in the VLD measurement of VDD_STS: VLDloss = 0.01

$$T_{sts\_period} = \frac{3 \cdot 10^{-9}}{4 \cdot 2 \cdot 10^{-6} \cdot 0.01} = 37.5 \cdot 10^{-3}$$

Equation 7: Example of STS Survey Period Calculation

According to the Table 4, the closest value to 37.5ms is 32ms, corresponding to *reg_t_sts_period* = “100”. In that condition the power loss in the VLD would be about 1.2%.

8 HYSTERESIS ON V_BAT_MIN SETTINGS

The voltage level **v_bat_min_hi** defines an hysteresis with **v_bat_min_lo**. It has a particular importance to supervise STS when VDD_STS and VDD_LTS are disconnected; in primary cell mode or when VDD_LTS falls below **v_bat_min_lo**.

8.1 Level v_bat_min_hi with VDD_STS and VDD_LTS disconnected

The level **v_bat_min_hi** is set by the register *reg_v_bat_min_hi_dis* when VDD_STS and VDD_LTS are disconnected. When the EM8500 DCDC converter does not charge Csts and VDD_STS and VDD_LTS are disconnected, Csts is the only source of energy for the application. Depending on the current consumption of the application in that condition, Csts will drop more or less quickly. If VDD_STS falls below the level **v_bat_min_lo**, the EM8500 will stop supplying the application; it will disable VSUP and VAUX[i]. As soon as the VLD measures VDD_STS below **v_bat_min_hi_dis**, the EM8500 DCDC converter is enabled to recover VDD_STS as shown in the following figures:

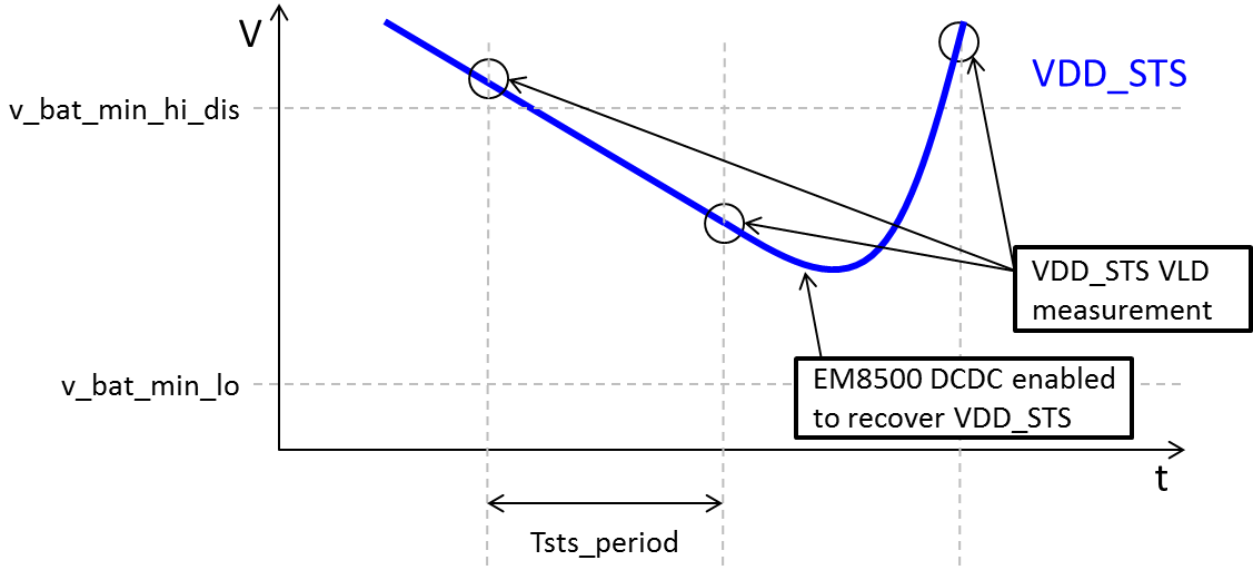

Figure 1: VDD_STS Measurement Toward v_bat_min_hi_dis

The voltage difference between v_bat_min_hi_dis and v_bat_min_lo shall be higher than the voltage drop on VDD_STS between 2 Tsts_period with the maximum current consumption. The following equation calculates **v_bat_min_hi_dis**:

$$v\_bat\_min\_hi\_dis = \frac{2 \cdot T_{sts\_period} \cdot I_{max}}{C_{sts}} + v\_bat\_min\_lo$$

Equation 8: v_bat_min_hi_dis Calculation

Imax (in [A]) is the maximum current consumption on application side.
Tsts_period (in [s]) is the period between 2 VDD_STS VLD measurements defined in chapter 7.
Csts (in [F]) is the capacitor connected to VDD_STS.

8.2 Example of v_bat_min_hi_dis calculation

Considering that Tsts_period is 32ms, Csts is 100uF, the maximum consumption of the application is 1mA and the absolute minimum battery voltage is 1.2V. According to the Equation 8, the value of **v_bat_min_hi_dis** shall be at least 1.84V.
The register *reg_v_bat_min_hi_dis* is calculated as follows:

$$reg\_v\_bat\_min\_hi\_dis = \mathrm{trunc}\left(\frac{v\_bat\_min\_hi\_dis}{\max(V_{lvl})} - 1\right) + 1$$

Equation 9: Register *reg_v_bat_min_hi_dis* Calculation

In our example the value of *reg_v_bat_min_hi_dis* = 24 (0x18 in hexadecimal)

8.3 Level v_bat_min_hi with VDD_STS and VDD_LTS connected

The level **v_bat_min_hi** is set by the register *reg_v_bat_min_hi_con* when VDD_STS and VDD_LTS are connected. This level defines a hysteresis with **v_bat_min_lo**. As LTS has a huge capacity compare to Csts, this parameter is less crucial than **v_bat_min_hi_dis**. This hysteresis delimitates the VDD_LTS voltage range wherein the flag BAT_LOW is set to '1' before stopping the supply of the application (disabling VSUP and VAUX[i]).
The difference between **v_bat_min_hi_con** and **v_bat_min_lo** is depending on the battery discharge curve. There is only one strict rule:

$$reg\_v\_bat\_min\_hi\_con \geq reg\_v\_bat\_min\_lo + 1$$

Equation 10: *reg_v_bat_min_hi_con* Toward *reg_v_bat_min_lo Conditions*

9 LEVEL V_APL_MAX_LO SETTINGS

As already written in chapter 5.2, the levels **v_apl_max_lo** and **v_apl_max_hi** shall be set to 0x3F if the application can afford the absolute maximum battery voltage. In that condition, these two levels are ignored. If it is not the case, and if VDD_STS and VDD_LTS are disconnected, the level **v_apl_max_lo** calculation shall fulfill 2 conditions:

1. The difference between **v_apl_max_lo** and **v_bat_min_hi_dis** shall be enough high to let the EM8500 DCDC charging LTS a minimum of time.
2. The hysteresis between **v_apl_max_lo** and **v_apl_max_hi** shall be enough high to ensure VDD_STS will never rise above **v_apl_max_hi**.

9.1 Level v_apl_max_lo toward v_bat_min_hi

When VDD_LTS and VDD_STS are disconnected, the EM8500 DCDC charges alternatively STS and LTS. When the VLD detects that STS reached **v_apl_max_lo**, the EM8500 DCDC stops charging STS and starts charging LTS. In that condition STS is the only source of energy of the application. It drops down to **v_bat_min_hi_dis** and then the EM8500 charges back STS. To charge the battery in an efficient way, the period during which the EM8500 DCDC charges LTS shall be as long as possible.

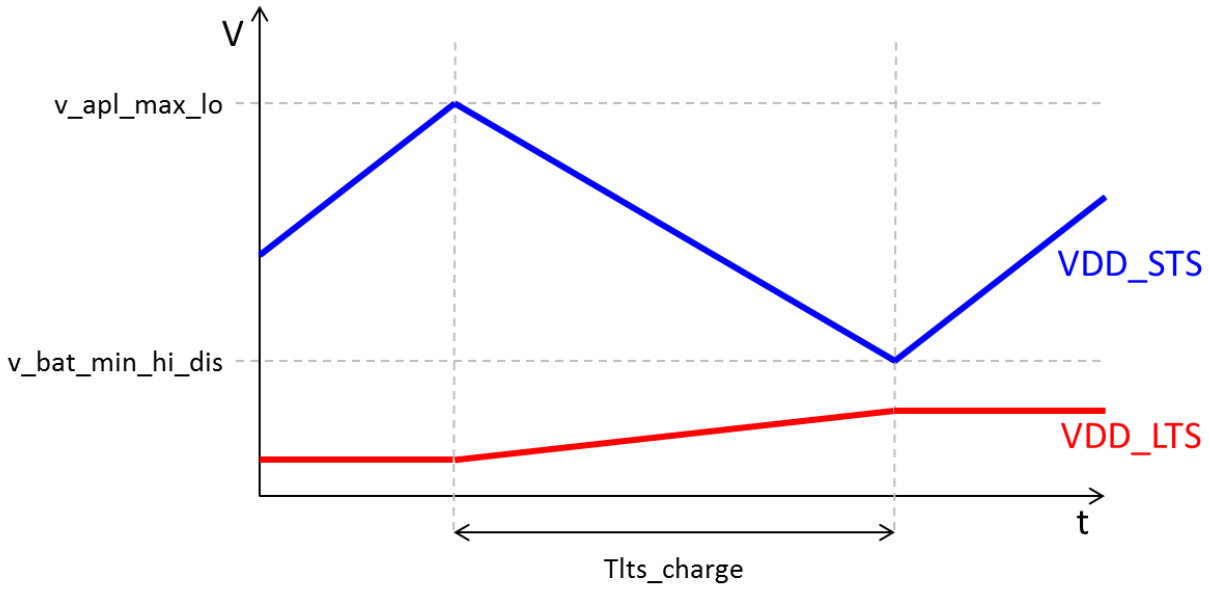

Figure 2: Effect of v_apl_max_lo Level on VDD_LTS Charge Phase Period

Considering Tlts_charge_min is the minimum period we want to guarantee, the condition **v_apl_max_lo** level shall fulfill toward **v_bat_min_hi_dis** is the following:

$$v\_apl\_max\_lo \geq \frac{T_{lts\_charge\_min} \cdot I_{max}}{C_{sts}} + v\_bat\_min\_hi\_dis$$

Equation 11: v_apl_max_lo toward v_bat_min_hi_dis Condition

9.2 Level v_apl_max_lo toward v_apl_max_hi

When the EM8500 DCDC charges STS at full power, VDD_STS rising edge can be sharp and therefore, depending on Tsts_period, rise above **v_apl_max_hi** if there is not enough hysteresis between **v_apl_max_lo** and **v_apl_max_hi**.

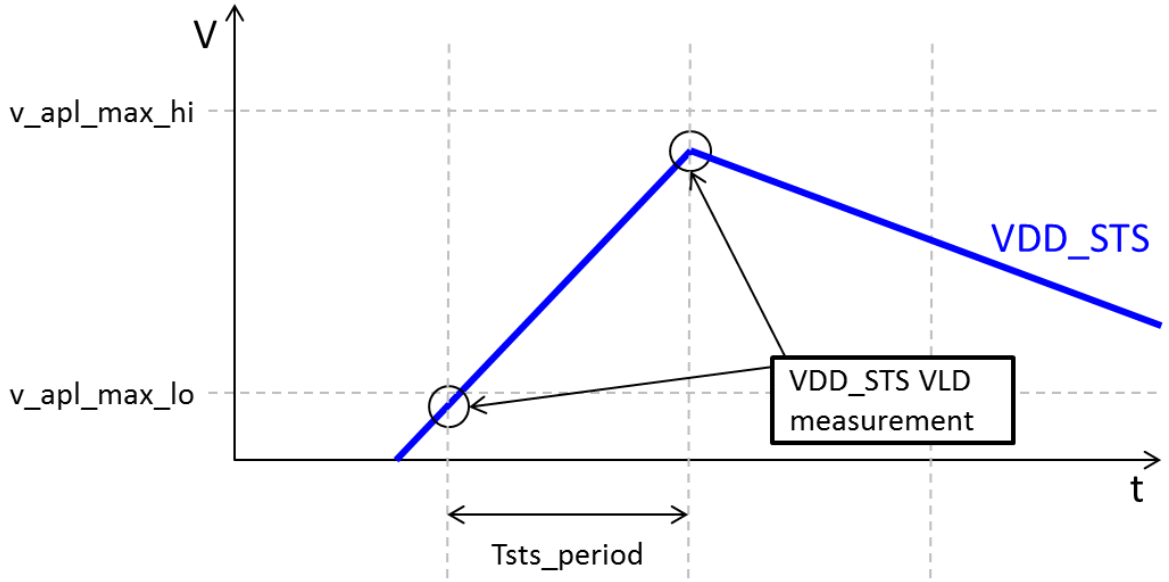

Figure 3: VDD_STS Measurement Toward v_apl_max_lo

The sharpness of VDD_STS rising edge is depending on the maximum power the EM8500 DCDC can harvest. To have enough margins, we consider that the EM8500 DCDC has an ideal efficiency of 100%. When the EM8500 DCDC converter charges STS, the maximum power that the EM8500 DCDC can deliver is limited even if the HRV can potentially deliver more power (when charging LTS there is no such limitation). The maximum power Pin_max that the DCDC converters can deliver to STS depends mainly on Vmpp in best case conditions, meaning at maximum luminescence for a solar cell for instance. Pin_max is calculated as follows:

$$P_{in\_max} = 6.65 \cdot 10^{-3} \cdot Vmpp^2$$

Equation 12: Pin_max Caclulation

Note: the chapter 2 of the document *e8500_app_note_hrv_param.pdf* describes how to calculate Vmpp.
The level **v_apl_max_lo** shall fulfill the following equation to ensure VDD_STS will never rise above **v_apl_max_hi** when the DCDC converter charges STS.

$$v\_apl\_max\_lo < \sqrt{v\_apl\_max\_hi^2 - \frac{4 \cdot T_{sts\_period} \cdot P_{in\_max}}{C_{sts}}}$$

Equation 13: v_apl_max_lo toward v_apl_max_hi Condition

9.3 Level v_apl_max_lo adjustment

The level **v_apl_max_lo** shall fulfill both Equation 11 and Equation 13. If it is not the case, there are two main ways to correct it:

1. Reduce Tsts_period: it impacts the efficiency at very low power range; it is in the majority of the cases negligible. The value of VLDloss shall be reconsidered in Equation 6.
2. Increase Csts: it can impacts the mechanical size of the component and its cost. The solution 1 is preferable.

9.4 Level v_apl_max_lo with VDD_STS and VDD_LTS connected

If VDD_LTS and VDD_STS are **always** connected, the calculation of **v_apl_max_lo** is less critical and shall only fulfill the following rule:

$$reg\_v\_apl\_max\_lo \leq reg\_v\_apl\_max\_hi - 1$$

Equation 14: *reg_v_apl_max_lo* toward *reg_v_apl_max_hi* Condition

10 LEVEL V_BAT_MAX_LO SETTINGS

If the application can afford the maximum battery voltage, **v_apl_max_lo** and **v_apl_max_hi** are set to 0x3F and respectively 0x3E and not used. In that case, the conditions defined by the Equation 11 and Equation 13 shall be applied to **v_bat_max_lo** as follows:

$$\frac{T_{lts\_charge\_min} \cdot I_{max}}{Csts} + v\_bat\_min\_hi\_dis \leq v\_bat\_max\_lo < \sqrt{v\_bat\_max\_hi^2 - \frac{4 \cdot T_{sts\_period} \cdot P_{in\_max}}{C_{sts}}}$$

Equation 15: v_bat_max_lo Conditions; v_apl_max_lo and v_apl_max_hi not Used

If both conditions of Equation 15 cannot be fulfilled, the corrective actions are the same then the one defined in chapter 9.3.

10.1 Level v_bat_max_lo with VDD_STS and VDD_LTS connected

If VDD_LTS and VDD_STS are **always** connected or if **v_apl_max_lo** and **v_apl_max_hi** are used, the calculation of **v_bat_max_lo** is less critical and shall only fulfill the following rule:

$$reg\_v\_bat\_max\_lo \leq reg\_v\_bat\_max\_hi - 1$$

Equation 16: *reg_v_bat_max_lo* toward *reg_v_bat_max_hi* Condition

11 LTS SURVEY PERIOD

As LTS is huge compare to STS, the LTS survey period **Tlts_period** is not critical at all. It could be set to a high value without any impact. The power consumption of LTS survey, when **Tlts_period** is 1s, is less than 1nW. In HRV_LOW mode, this period (**Tlts_period_hrv_low**) is set by *reg_t_hrv_low_cfg.t_lts_hrv_low_period* to a different value, but as in operating the impact is negligible. We advise the user to set **Tlts_period** to 1s and **Tlts_period_hrv_low** to 2s as follows:
reg_t_lts_period = 101
reg_t_hrv_low_cfg.t_lts_hrv_low_period = 101
Tlts_period is set by the registers *reg_t_lts_period* and *reg_t_hrv_low_cfg.t_lts_hrv_low_period* as follows:

Reg value	Tlts_period register : *reg_t_lts_period*	Tlts_period in HRV_LOW mode register : *reg_t_hrv_low_cfg.t_lts_hrv_low_period*
000	1ms	2ms
001	4ms	8ms
010	16ms	32ms
011	64ms	128ms
100	256ms	512ms
101	1s	2s
110	4s	8s
111	16s	32s

Table 5: Tlts_period and Tlts_period_hrv_low Related Registers Selection

Note: At start-up the EM8500 waits **Tlts_period** before to enable VSUP. Usually this is not critical as the start-up is executed one time in the life of the product.

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