SUPPLY OUTPUTS VSUP / VAUX / VAUX_GND CONTROL

Product Family: **EM850X**

Part Number: EM8500

Keywords: Harvesting, Solar, TEG, MPPT, Configuration, Setup, Super capacitors, Secondary Battery, Primary Battery, LDO

ABSTRACT

The EM8500 offers a NVM containing all the configuration parameters. This document describes how to setup the registers in NVM linked to the control of the supply outputs VSUP, VAUX[2:0], VAUX_GND[2:0]:

- Enable and disable the supply outputs
- Configure direct or regulated supply outputs
- Configure the sleep mode and wake-up system
- Configure the supply outputs behavior in HRV_LOW mode

ABBREVIATIONS

NVM	Non-Volatile-Memory
MCU	Microcontroller Unit
STS	Short term storage element (capacitor connected to VDD_STS)
LTS	Long term storage element (rechargeable battery connected to VDD_LTS)
HRV	Harvester, main source of energy (solar or TEG)
TEG	Thermal Electrical Generator
BAT_LOW	Flag indicating that the battery is in under-voltage condition
HRV_LOW	Flag indicating that the HRV is under the minimum power level (HRV low mode when at 1)
VSUP	Main output supply for application
VAUX[*i*]	3 independent auxiliary supplies for application (*i* is in the range 0 to 2)
VAUX_GND[*i*]	3 independent switches to ground (*i* is in the range 0 to 2)
ULP LDO	LDO dedicated to VSUP
v_ulp_ldo	ULP LDO voltage level in [V]
VAUX LDO	LDO common to all VAUX[*i*]
v_aux_ldo	VAUX LDO voltage level in [V]
Csup	Decoupling capacitor on VSUP
Caux[*i*]	3 decoupling capacitors on VAUX[*i*] (*i* is in the range 0 to 2)
Sleep	VSUP is disabled when the sleep mode is active
v_apl_max_hi	Absolute maximum application voltage
v_apl_max_lo	Maximum voltage of the application, form an hysteresis with **v_apl_max_hi**
v_bat_min_hi	Minimum battery and application voltage define by **v_bat_min_hi_dis** when STS and LTS are disconnected; otherwise it is defined by **v_bat_min_hi_con**. It forms an hysteresis with **v_bat_min_lo**.
v_bat_min_lo	Absolute minimum value of the battery and the application

1 SCOPE

The EM8500 generates 4 supply outputs for external application:

- VSUP: main supply output, used usually to supply the main MCU
  - Can be directly connected to VDD_STS or regulated by ULP_LDO
  - Can be configured to be disabled in HRV_LOW mode
  - Can be disabled (sleep mode) for a predefine duration
  - Wake-up pin can force VSUP out of sleep mode
  - Can be configured to be tied to ground or floating when disabled
- VAUX[*i*]: 3 independent supply outputs for peripherals such as RF transmitters, sensors etc...
  - Can be directly connected to VDD_STS or regulated independently by VAUX LDO
  - Can be configured to be disabled in HRV_LOW mode independently
  - Can be disabled / enabled independently
  - Can be configured to be tied to ground or floating when disabled independently
- VAUX_GND[*i*]: 3 independents switches to ground
  - Can cut the ground of a peripheral; for instance to avoid current leakage through the pull-up of an I^2C line
  - Can be disabled / enabled independently

The following registers are involved for that action:

Register name	Address	Description
reg_ldo_cfg	0x0E	*vsup_tied_low*: In sleep mode VSUP is connected to ground if vsup_tied_low = '1' In sleep mode VSUP is floating if vsup_tied_low = '0' *v_vaux_ldo[2:0]*: Regulation level of VAUX LDO *frc_ulp_ldo*: VSUP is always regulated by ULP_LDO when enabled *v_ulp_ldo[2:0]*: Regulation level of ULP_LDO
reg_pwr_cfg	0x0F	*dis_vaux_gnd[i]_hrv_low*: VAUX_GND[*i*] is disabled in HRV_LOW mode when at '1' *dis_vaux[i]_hrv_low*: VAUX[*i*] is disabled in HRV_LOW mode when at '1' *dis_vsup_hrv_low*: VSUP is disabled in HRV_LOW mode when at '1'
reg_vaux_cfg	0x10	*vaux[i]_cfg[1:0]*: When "00": Configure VAUX[*i*] to be connected to VDD_STS when enabled When "01": Configure VAUX[*i*] to be connected to VAUX LDO when enabled When "10": Configure VAUX[*i*] to be connected to VAUX LDO only when VDD_STS is above **v_apl_max_hi**, VAUX[*i*] is floating when disabled When "11": Configure VAUX[*i*] to be connected to VAUX LDO only when VDD_STS is above **v_apl_max_hi**, VAUX[*i*] is connected to ground when disabled
reg_vaux_gnd_cfg	0x11	*vaux_gnd[i]_cfg*: When '0': Configure VAUX_GND[*i*] to be always connected to ground when enabled When '1': Configure VAUX_GND[*i*] to be connected to ground only when enabled and VDD_STS is lower than **v_apl_max_hi**

Register name	Address	Description
reg_ext_cfg	0x13	*wake_up_deb_en*: debouncer is connected to the pin wake-up when at '1' *wake_up_edge_cfg[1:0]*: When "00": wake-up pin is sensitive to no edge (wake-up disabled) When "01": wake-up pin is sensitive to the falling edge When "10": wake-up pin is sensitive to the rising edge When "11": wake-up pin is sensitive to the falling and the rising edges
reg_t_sleep_vsup_lo	0x14	Sleep wake-up counter duration coded over 3 bytes: *reg_t_sleep_vsup[23:0] = reg_t_sleep_vsup_hi & reg_t_sleep_vsup_mid & reg_t_sleep_vsup_lo*
reg_t_sleep_vsup_mid	0x15	
reg_t_sleep_vsup_hi	0x16	
reg_pwr_mgt	0x19	*frc_prim_dcdc_dis*: force the EM8500 DCDC off when at '1' *vaux_gnd[i]_en*: connects VAUX_GND[*i*] to ground when at '1' *vaux[i]_en*: enable VAUX supply when at '1' *sleep_vsup*: set VSUP in sleep mode when at '1'

Table 1: List of Registers Related to Supply Outputs Control

The default value after reset or start-up of the registers listed in 8 is contained in a NVM memory at the following related addresses:

Register name	Register Address	Related address in NVM	
reg_ldo_cfg	0x0E	eeprom14	0x4E
reg_pwr_cfg	0x0F	eeprom15	0x4F
reg_vaux_cfg	0x10	eeprom16	0x50
reg_vaux_gnd_cfg	0x11	eeprom17	0x51
reg_ext_cfg	0x13	eeprom19	0x53
reg_t_sleep_vsup_lo	0x14	eeprom20	0x54
reg_t_sleep_vsup_mid	0x15	eeprom21	0x55
reg_t_sleep_vsup_hi	0x16	eeprom22	0x56
reg_pwr_mgt	0x19	eeprom25	0x59

Table 2: Relation between Register and Corresponding NVM Address

Note: offset between the register addresses and related address in NVM is 0x40

2 VSUP SETTINGS

VSUP is the main supply output used to supply the main MCU of the application. VSUP is enabled by default and, with one exception, cannot be permanently disabled. The user can set VSUP in sleep mode; this action disables VSUP for a predefined duration to reduce the consumption of the system as much as possible. The pin wake-up stops the sleep mode at any time.
It is possible to permanently disable VSUP only in HRV_LOW mode. But we strongly advise never to use this option; the system can enter into a dead lock.
The voltage VDD_STS supplies VSUP directly or through the ULP LDO. The ULP LDO ensures that VSUP never rises above **v_apl_max_hi**. The user can force the ULP LDO even if VDD_STS is lower than **v_apl_max_hi**.

2.1 VSUP enable conditions

The EM8500 enables VSUP as soon as VDD_STS rises above **v_bat_min_hi** and disables VSUP when VDD_STS falls below **v_bat_min_lo**.

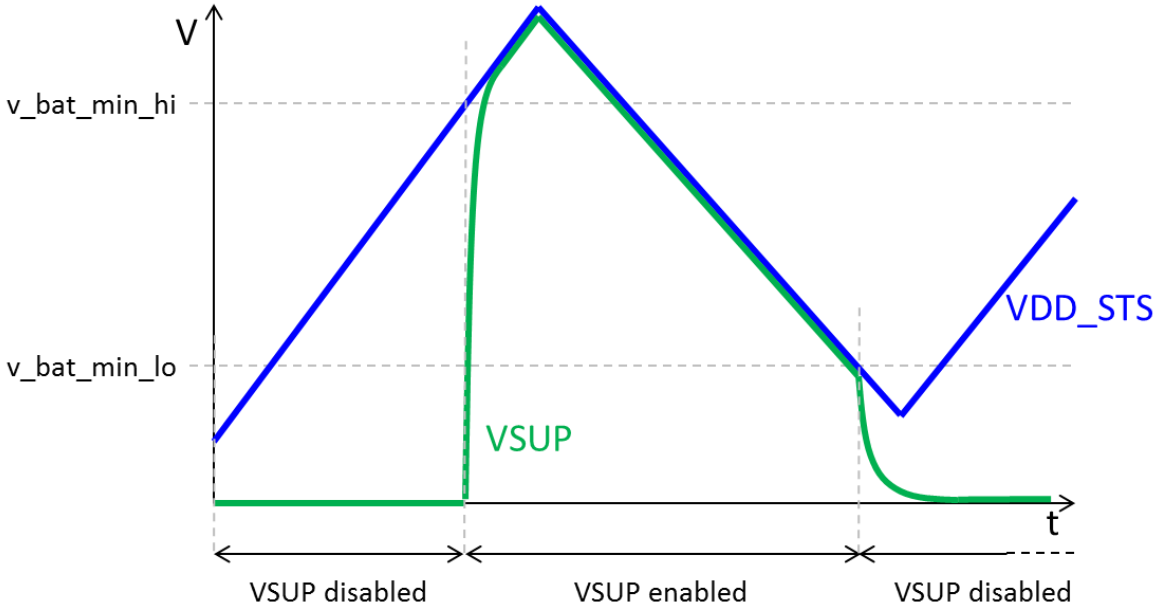

Figure 1: VSUP Enable Condition Dependence on VDD_STS

The following conditions also disable VSUP:

- In “VSUP sleep mode”, when the bit register *reg_pwr_mgt.sleep_vsup* is set to ‘1’
- The bit register *reg_pwr_cfg.dis_vsup_hrv_low* is set to ‘1’ and the EM8500 in HRV_LOW mode

2.2 VSUP disabled

If the register *reg_ldo_cfg.vsup_tied_low* = ‘1’, the EM8500 connects VSUP to the ground in disabled state, otherwise VSUP is floating in disabled state.
As shown in chapter 2.1, VSUP is disabled when *reg_pwr_cfg.dis_vsup_hrv_low* is set to ‘1’ and the EM8500 in HRV_LOW mode. This register shall be carefully handled, when it is at ‘1’ it is not possible to recover the supply output VSUP as long as there is no energy from the harvester. **We strongly advise never to set *reg_pwr_cfg.dis_vsup_hrv_low* to ‘1’.**

2.3 VSUP sleep mode

When the bit register *reg_pwr_mgt.sleep_vsup* is set to ‘1’, the EM8500 enters in “VSUP sleep mode” and disables VSUP and thus stops supplying the main application MCU. In such mode, a counter automatically starts and restores VSUP only when it reaches the value t_sleep_vsup set in the register *reg_t_sleep_vsup[23:0]*. This register is a concatenation of the 3 registers *reg_t_sleep_vsup_hi* & *reg_t_sleep_vsup_mid* & *reg_t_sleep_vsup_lo*:

$$reg\_t\_sleep\_vsup[23:0] = t\_sleep\_vsup[s] \cdot 1000$$

Equation 1: t_sleep_vsup Calculation

The maximum t_sleep_vsup duration is 0xFFFFFF * 1ms ≈ 4h 39min 37s.

2.4 Wake-up pin

The pin WAKE_UP restores VSUP from sleep mode and resets the sleep counter. It is possible to select on which edge the pin WAKE_UP is sensitive with the register *reg_ext_cfg.wake_up_edge_cfg[1:0]* as follows:

reg_ext_cfg.wake_up_edge_cfg[1:0]	**wake-up edge selection**
00	No edge (wake-up pin disabled)
01	Falling edge
10	Rising edge
11	Both edges

Table 3: WAKE_UP Edge Selection

The bit register *reg_ext_cfg.wake_up_deb_en* enables a debouncer on the pin WAKE_UP when it is at '1'. The state of WAKE_UP shall be stable during at least 171ms to take effect. If the debouncer is disabled, the latency of the pin WAKE_UP is 1us on the rising edge and 100us on the falling edge.

2.5 ULP LDO

The level **v_apl_max_hi** is the maximum value the application can afford. If VDD_STS rises above this level, the EM8500 disconnects VSUP from VDD_STS and enables the ULP LDO to regulate VSUP. To reduce the noise on VSUP or to get a stable DC voltage on VSUP, it is possible to force VSUP to always be connected to the ULP LDO. When the register *reg_ldo_cfg.frc_ulp_ldo* = '1', ULP LDO always regulates VSUP when it is enabled.
The register *reg_ldo_cfg.v_ulp_ldo[2:0]* selects the ULP LDO voltage level **v_ulp_ldo** as follows:

reg_ldo_cfg.v_ulp_ldo[2:0]	**v_ulp_ldo [V]**
000	1.2
001	1.55
010	1.65
011	1.8
100	2
101	2.2
110	2.4
111	2.6

Table 4: ULP LDO Voltage Level Selection

2.6 VSUP output capability

When VSUP is connected to VDD_STS, the connection through the switch has a typical resistor of 7.4Ohm.
The VSUP LDO has an output capability of 10mA at a maximum drop of 100mV.

3 VAUX SETTINGS

VAUX[2:0] are 3 independent supply outputs. They usually supply peripherals such as RF transmitter, sensors etc… The user can set each of them independently to be disabled, connected to VDD_STS or regulated by the common VAUX LDO.

3.1 VAUX enable conditions

The user can enable any VAUX[*i*] as soon as VDD_STS rises above **v_bat_min_hi**. The EM8500 disables all VAUX[2:0] when VDD_STS falls below **v_bat_min_lo**.

- Setting the register *reg_pwr_mgt.vaux0_en* to '1' enables VAUX[0]
- Setting the register *reg_pwr_mgt.vaux1_en* to '1' enables VAUX[1]
- Setting the register *reg_pwr_mgt.vaux2_en* to '1' enables VAUX[2]

Each VAUX[*i*] can be configured independently with the register *reg_vaux_cfg.vaux[i]_cfg[1:0]* as follows:

reg_vaux_cfg.vaux[i]_cfg[1:0]	**v_ulp_ldo [V]**
00	Connect VAUX[*i*] to VDD_STS when enabled
01	Connects VAUX[*i*] to VAUX LDO when enabled
10	Connect VAUX[*i*] automatically to VAUX LDO when VDD_STS is above **v_apl_max_hi**, VAUX[*i*] is floating when disabled
11	Configure VAUX[*i*] to be connected to VAUX LDO only when VDD_STS is above **v_apl_max_hi**, VAUX[*i*] is connected to ground when disabled

Table 5: VAUX[*i*] Configuration

When the register *reg_pwr_cfg.dis_vaux[i]_hrv_low* = '1', the related VAUX[*i*] is automatically disabled when the EM8500 is in HRV_LOW mode.

3.2 VAUX LDO

Unlike VSUP, VAUX can be connected to VDD_STS even if VDD_STS is above **v_apl_max_hi** as defined in Table 5. The VAUX LDO is common to all VAUX[2:0], but each VAUX[*i*] can be independently connected to VAUX LDO. The register *reg_ldo_cfg.v_vaux_ldo[2:0]* selects the VAUX LDO voltage level **v_aux_ldo** as follows:

reg_ldo_cfg.v_vaux_ldo[2:0]	**v_aux_ldo [V]**
000	1.2
001	1.55
010	1.65
011	1.8
100	2
101	2.2
110	2.4
111	2.6

Table 6: VAUX LDO Voltage Level Selection

4 VAUX_GND SETTINGS

When VAUX[*i*] supplies a peripheral it could be necessary to cut the connection to the ground of that peripheral when VAUX[*i*] is disabled. In particular, if VSUP communicates with that peripheral through an I2C interface, it avoids drawing a current from the pull-up resistor into the peripheral.

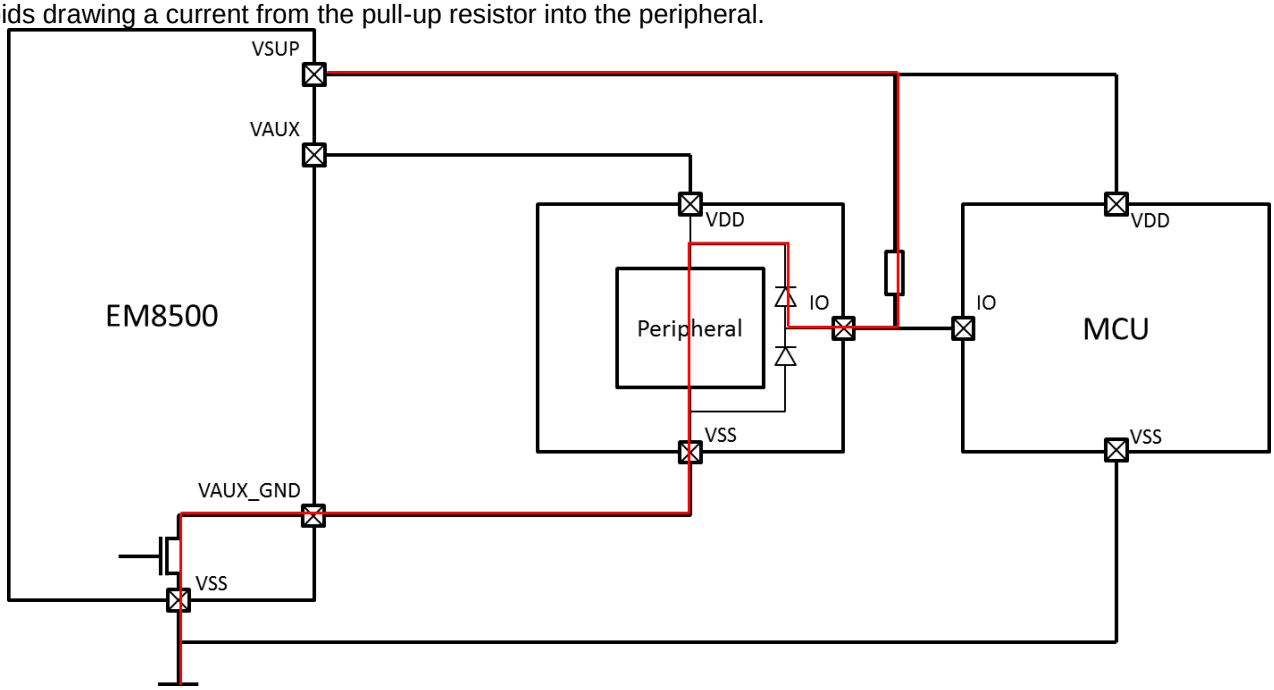

Figure 2: Peripheral Supplied Through IO Protection Diodes

In the Figure 2, if VAUX_GND is connected to the ground, the peripheral is supplied through the pull-up and the positive protection diode of IO pad, when VAUX is disabled. If VAUX_GND is disabled, no current can flow through that path.

4.1 VAUX_GND enable conditions

The user can enable any VAUX_GND[*i*] as soon as VDD_STS rises above **v_bat_min_hi**. The EM8500 disables all VAUX_GND[2:0] when VDD_STS falls below **v_bat_min_lo**.

- Setting the register *reg_pwr_mgt.vaux_gnd0_en* to '1' connects VAUX_GND[0] to VSS
- Setting the register *reg_pwr_mgt.vaux_gnd1_en* to '1' connects VAUX_GND[1] to VSS
- Setting the register *reg_pwr_mgt.vaux_gnd2_en* to '1' connects VAUX_GND[2] to VSS

Each VAUX_GND[*i*] can be configured independently with the register *reg_vaux_gnd_cfg.vaux_gnd[i]_cfg* as follows:

reg_vaux_gnd_cfg.vaux_gnd[i]_cfg	**v_ulp_ldo [V]**
0	Connect VAUX_GND[*i*] to ground even if VDD_STS is above **v_apl_max_hi** when enabled
1	Disconnect VAUX_GND[*i*] when VDD_STS is above **v_apl_max_hi** when enabled

Table 7: VAUX_GND[*i*] Configuration

When the register *reg_pwr_cfg.dis_vaux_gnd[i]_hrv_low* = '1', the related VAUX_GND[*i*] is automatically disabled when the EM8500 is in HRV_LOW mode.

5 NOISE REDUCTION

The EM8500 DCDC generates noise that can disturb sensitive devices such as sensors. Setting the register *reg_pwr_mgr.frc_prim_dcdc_dis* to '1' will stop the DCDC conversion.
If VDD_STS falls below **v_bat_min_hi**, the register *reg_pwr_mgr.frc_prim_dcdc_dis* is automatically reset to '0', thus the DCDC is reactivated.

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