

## 3V Self Recovering Watchdog

### Description

The H6061 is a combined initialiser, watchdog and voltage monitor. The circuit is a low voltage low power monolithic CMOS device combining a series of voltage comparators and a programmable timer on the same chip. The device is specially suited to telecommunications applications where 3 V working is expected, for functions such as supply voltage and microprocessor monitoring. The reset outputs are self recovering after a watchdog timeout, enabling the circuit to work with standalone systems without any external push-switch or control signal to restart after a watchdog timeout. The circuit provides a reset signal of both polarities. The state of the outputs is defined down to 1.6 V. An internal debouncer ensures power-up performance for fast-rise supply lines.

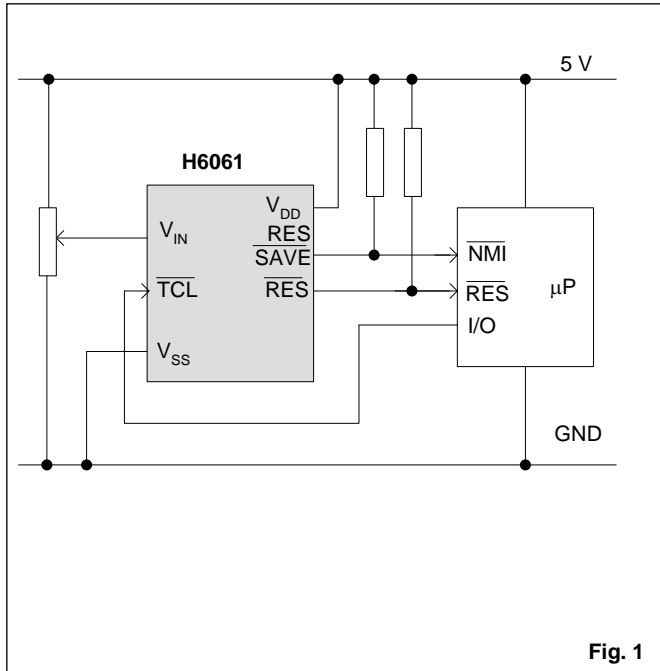
### Features

- Watchdog fully operational from 2.7 to 5.25 V
- Regulated DC voltage monitor, internal voltage reference
- Self recovering watchdog function: reset goes active after the 1st timeout period, reset goes inactive again after the 2nd timeout period, repeated active reset signal until the system recovers
- Standard timeout period and power-on reset time (100 ms), externally programmable from 3 ms to 3 mins if required
- Works down to 1.6 V supply voltage
- Low voltage alarm prior to reset on power-down
- Reset outputs of both polarities
- Open drain outputs
- SO8 package

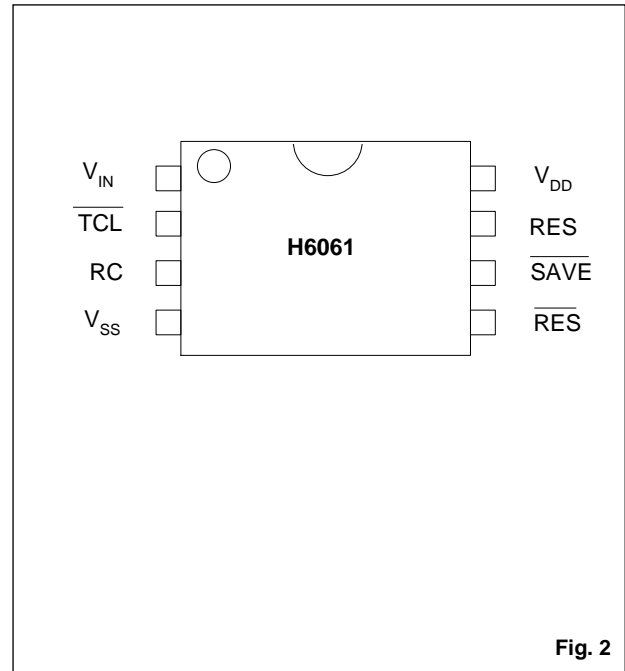
### Applications

- Microprocessor and microcontroller systems
- Point of sales equipment
- Telecom products
- Automotive subsystems
- Microcontroller 68HC05 applications

### Typical Operating Configuration



### Pin Assignment



**Absolute Maximum Ratings**

Parameter	Symbol	Conditions
Voltage $V_{DD}$ to $V_{SS}$	$V_{DD}$	- 0.3 to + 5.6 V
Voltage at any pin to $V_{SS}$	$V_{MIN}$	- 0.3
Voltage at any pin to $V_{DD}$	$V_{MAX}$	+ 0.3
Voltage at $V_{IN}$ to $V_{SS}$	$V_{INMAX}$	+ 12 V
Current at any output	$I_{MAX}$	$\pm 10$ mA
Storage temperature	$T_{STO}$	-65°C to +150°C
Electrostatic discharge max. to MIL-STD-833C method 3014	$V_{Smax}$	1000V

**Table 1**

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

**Handling Procedures**

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

**Operating Conditions**

Parameter	Symbol	Min.	Max.	Units
Operating temperature Industrial	$T_{AI}$	-40	+85	°C
Supply voltage	$V_{DD}$	2.7	5.25	V
Version 11,12	$V_{IN}$	0	12	V
RC-oscillator programming				
External capacitance*	C1		1	$\mu$ F
External resistance	R1	10		k $\Omega$

\* Leakage < 1  $\mu$ A

**Table 2**
**Electrical Characteristics**

$V_{DD} = 5.0$  V,  $T_A = -40$  to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
$V_{DD}$ activation threshold	$V_{ON}$	$T_A = 25$ °C	2.3		2.7	V
$V_{DD}$ deactivation threshold	$V_{OFF}$	$T_A = 25$ °C		$V_{ON}-0.3$		V
Supply current Input $V_{IN}$ , $\overline{TCL}$	$I_{DD}$	RC open, $\overline{TCL}$ at $V_{DD}$ or $V_{SS}$		80	140	$\mu$ A
Leakage current	$I_P$	$V_{SS} < V_{IP} < V_{DD}$ $T_A = 80$ °C		0.005	1	$\mu$ A
$\overline{TCL}$ input low level	$V_{IL}$				0.8	V
$\overline{TCL}$ input high level	$V_{IH}$		2.4			V
Leakage on pins $\overline{SAVE}$ , $\overline{RES}$ , RES	$I_{OLK}$	$V_{OUT} = V_{DD}$		0.050	1	$\mu$ A
O/P drive logic low	$I_{OL}$	$V_{OL} = 0.4$ V	4	8		mA
	$I_{OL}$	$V_{DD} = 3.5$ V; $V_{OL} = 0.4$ V	2			mA
	$I_{OL}$	$V_{DD} = 1.6$ V; $V_{OL} = 0.4$ V	80			$\mu$ A

**Table 3**
 **$V_{IN}$  Surveillance**

Voltage thresholds at  $T_A = 25$  °C

Version No.	Thresholds			at $V_{DD}$	Threshold Voltage Tolerance	Threshold Ratio*	Pin $V_{IN}$ Input
	$V_{SH}$	$V_{SL}$	$V_{RL}$				
25	1.54	1.50	1.46	2.7 – 5.0 V	$\pm 10\%$	$\pm 2\%$	$\sim 100$ M $\Omega$

\* Threshold ratio defined as  $V_{SH} / V_{SL}$  or  $V_{SL} / V_{RL}$ .

**Table 4**
**Timing Characteristics**

$V_{DD} = 5.0$  V,  $T_A = -40$  °C to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays $\overline{TCL}$ to output pins	$T_{DIDO}$			250	500	ns
$V_{IN}$ to output pins	$T_{AIDO}$	Excluding debounce time $T_{DB}$		4	10	$\mu$ s
Logic transition times on all output pins	$T_{TR}$	Load 10 k $\Omega$ , 100 pF		30	100	ns
Timeout period	$T_{TO}$	RC open, unshielded, $T_A = 25$ °C	60	100	160	ms
$\overline{TCL}$ input pulse width	$T_{TCL}$		150			ns
Power-on reset debounce	$T_{DB}$			$T_{TO}/64$		ms
Fastest pulse $V_{IN}$ with debounce	$T_{VINL}$	-40 to +85 °C	10			$\mu$ s

**Table 5**

**Timing Waveforms**  
**Voltage Reaction:  $V_{DD}$**   
**Monitoring**

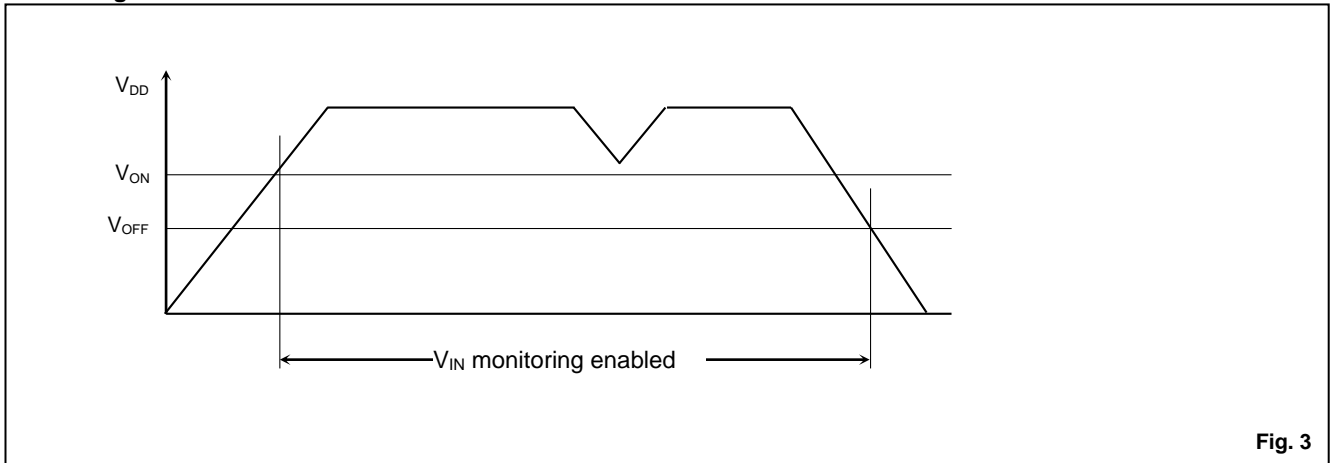
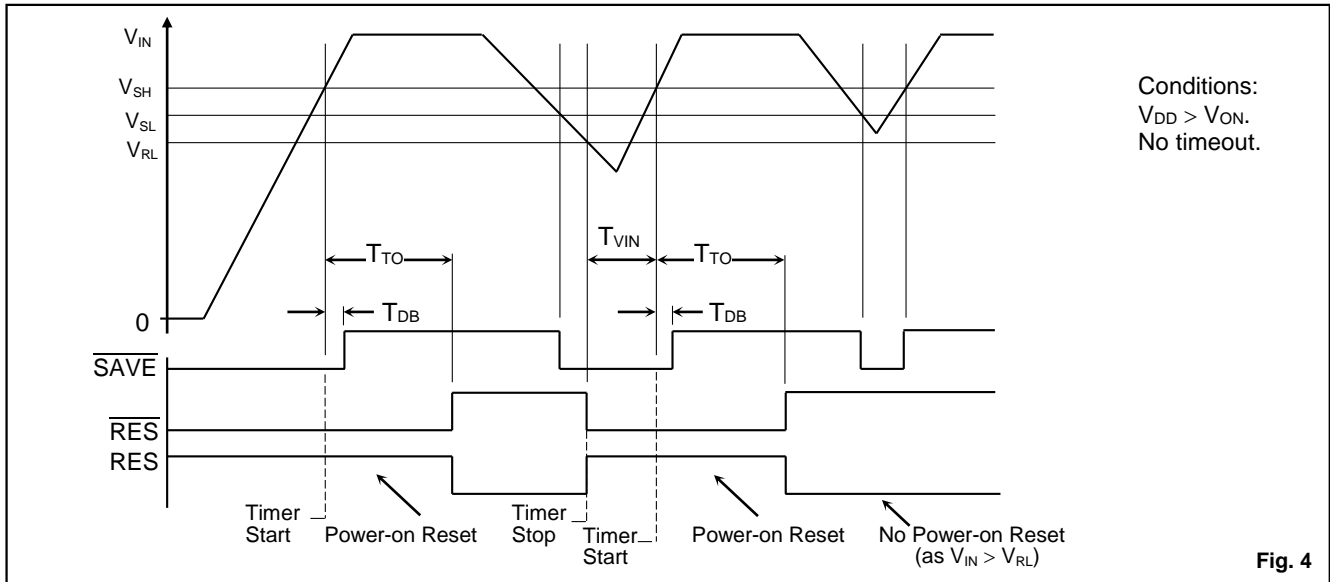


Fig. 3

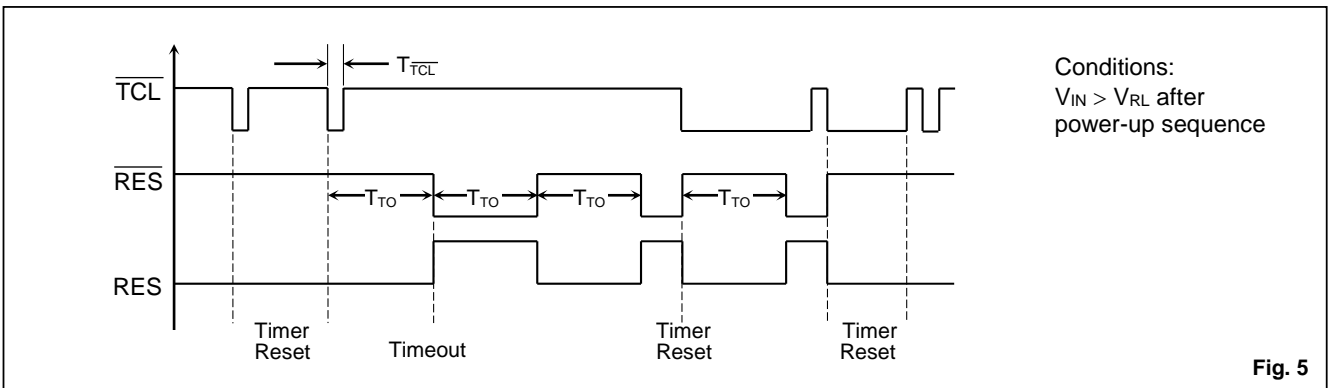
**Voltage Reaction:  $V_{IN}$  Monitoring**



Conditions:  
 $V_{DD} > V_{ON}$ .  
 No timeout.

Fig. 4

**Timer Reaction**



Conditions:  
 $V_{IN} > V_{RL}$  after  
 power-up sequence

Fig. 5

**Combined Voltage and Timer Reaction**

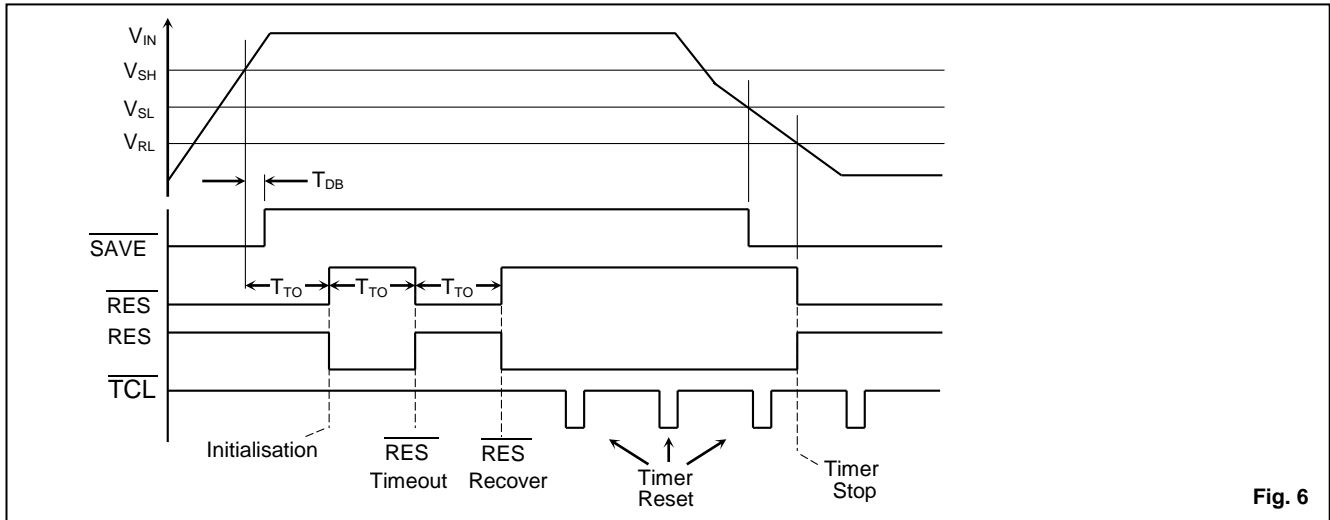


Fig. 6

**Block Diagram**

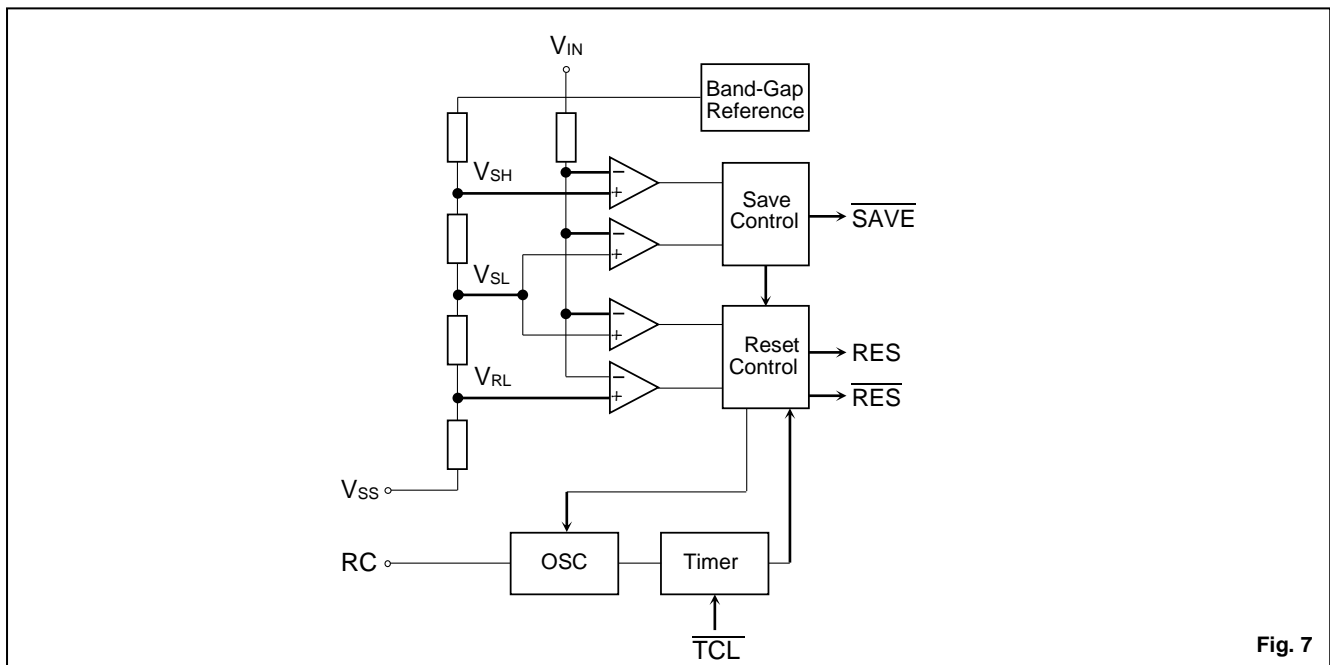


Fig. 7

**Pin Description**

Pin	Name	Function
1	V <sub>IN</sub>	Voltage monitoring input
2	$\overline{\text{TCL}}$	Timer clear input signal
3	RC	RC oscillator tuning input
4	V <sub>SS</sub>	GND terminal
5	$\overline{\text{RES}}$	Reset output, open drain
6	$\overline{\text{SAVE}}$	Save output, open drain
7	RES	Positive reset output, open drain
8	V <sub>DD</sub>	Positive supply voltage

**Table 6**
**Functional Description**
**Thresholds and Outputs**

The H6061 has open-drain outputs and voltage thresholds on pin V<sub>IN</sub> of typically 1.5 V.

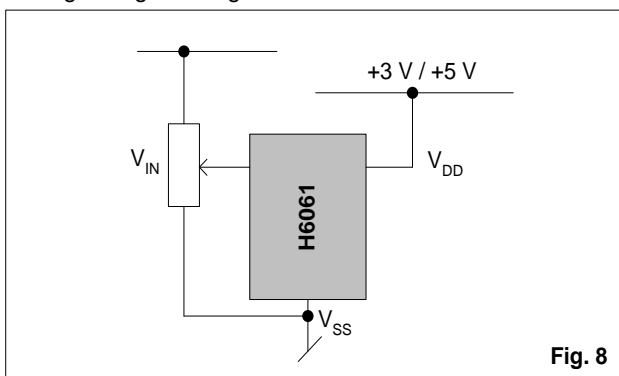
**Internal Voltage Comparators**

The voltage comparators detect the voltage applied to pin V<sub>IN</sub> and compare it with thresholds V<sub>SH</sub>, V<sub>SL</sub> and V<sub>RL</sub>. The H6061 is designed for monitoring regulated DC voltages and has bandgap thresholds independent of V<sub>DD</sub>. The reaction of the H6061 to voltage changes on pin V<sub>IN</sub> is given in Fig. 4. During powering-up, the outputs are active. After V<sub>IN</sub> reaches the V<sub>SH</sub> level, pin  $\overline{\text{SAVE}}$  deactivates after a short debounce time T<sub>DB</sub> to allow for fast ramp-ups. The initialization time T<sub>TO</sub> then passes before the two reset outputs go inactive. Thereafter, when the voltage on pin V<sub>IN</sub> falls below the V<sub>SL</sub> level, pin  $\overline{\text{SAVE}}$  goes active low as a first warning. If V<sub>IN</sub> then drops below the V<sub>RL</sub> level, the reset signals go active and are guaranteed down to 1.6 V. The reset outputs react also to timeouts (see “Timer clearing”). Note that when the supply voltage V<sub>DD</sub> is below the level V<sub>OFF</sub> (about 2.2 V), all outputs are in the active state for any allowed voltage of V<sub>IN</sub>.

**Voltage Programming**

The H6061 was designed to give the best compromise in normal usage (see Table 3). Its voltage threshold can be programmed by an external resistor divider or a potentiometer to react at proportionally higher voltage levels (see Fig. 8 below).

Voltage Programming


**Fig. 8**
**Timer Programming**

A single timeout period T<sub>TO</sub> is used for the initialization reset duration and the watchdog timeout. With pin RC unconnected, the on-chip RC oscillator and divider chain give a timeout period T<sub>TO</sub> of typically 100 ms. A resistor to V<sub>DD</sub> will shorten this time, and a capacitor to V<sub>SS</sub> will lengthen it (see Fig. 11). An approximation for calculating trial values given in milliseconds by the formula:

$$T_{TO} = \left[ 0.75 + \frac{(32 + C_1) \cdot 1.6}{V_{DD} - 0.8} \right] \cdot 8.192 \cdot \left[ 4.8 + \frac{V_{DD}}{R_1} \right]$$

$$R_1 \text{ min.} = 10 \text{ k}\Omega, C_1 \text{ max.} = 1 \text{ }\mu\text{F}$$

If R<sub>1</sub> is in M $\Omega$  and C<sub>1</sub> in pF, T<sub>TO</sub> will be in ms.

Choice of component values must be determined in practice. To have a square wave of period 2T<sub>TO</sub>, simply connect pin  $\overline{\text{TCL}}$  to V<sub>DD</sub> or V<sub>SS</sub> and take the signal output from a reset pin.

**Timer Clearing**

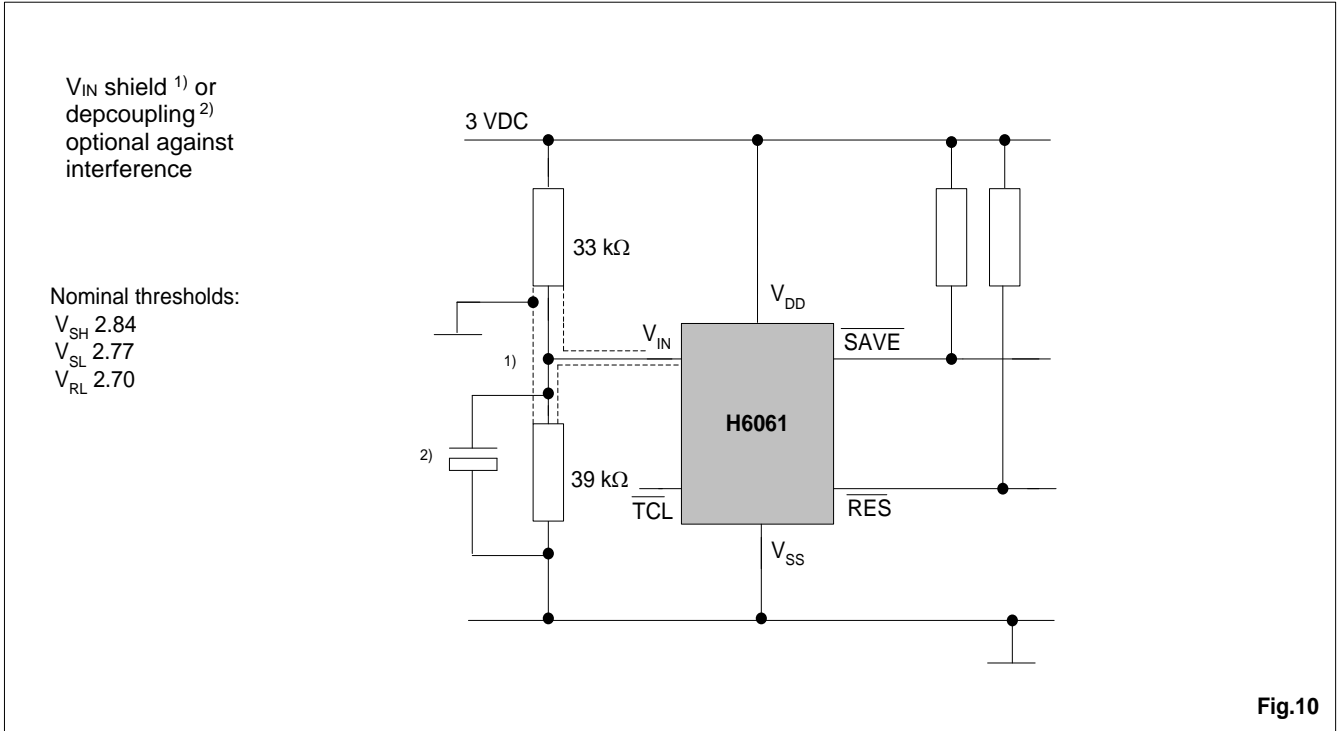
A negative edge or pulse at the  $\overline{\text{TCL}}$  input longer than 150 ns will clear the timer and deactivate the reset outputs under normal running conditions (see Fig. 3).  $\overline{\text{TCL}}$  will however have no effect either when V<sub>DD</sub> < V<sub>OFF</sub> or during the initialization period before the deactivation of the reset pins.

**Combined Voltage and Timer Action**

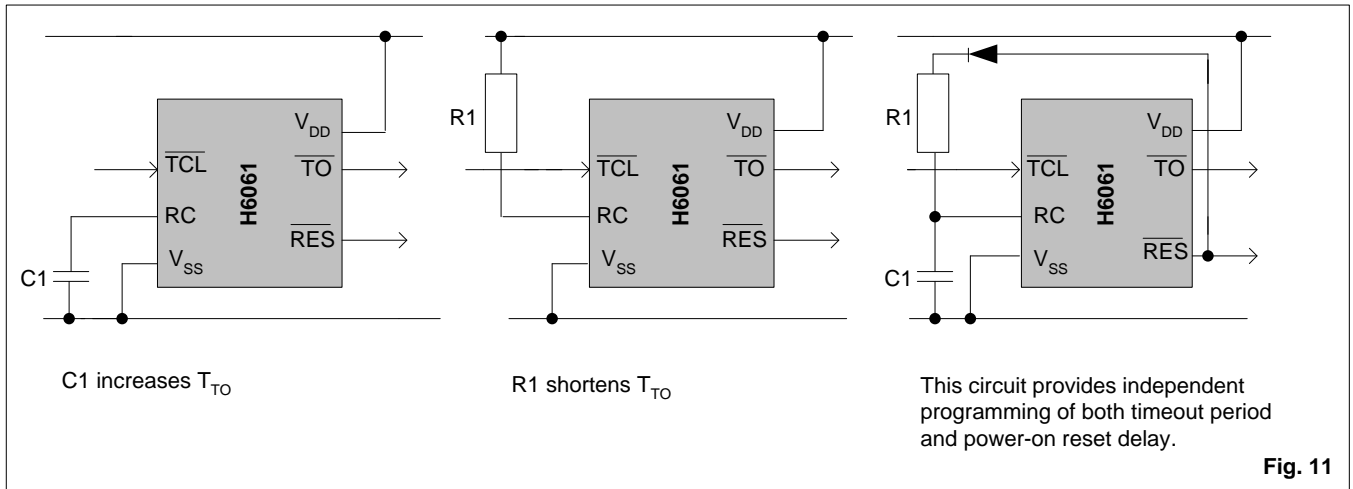
In Fig. 6 is a typical sequence of power-up, watchdog run, and power-down. During initialization the  $\overline{\text{SAVE}}$  pin deactivates one debounce delay time T<sub>DB</sub> after V<sub>IN</sub> rises above V<sub>SH</sub>, or when the power line V<sub>DD</sub> rises above V<sub>ON</sub>, whichever happens last. The reset pins only deactivate one timeout period T<sub>TO</sub> afterwards to free the watchdog timer and end the initialization. Note that either V<sub>IN</sub> falling below V<sub>RL</sub> threshold or V<sub>DD</sub> below V<sub>ON</sub> will cause an initialization upon recovery. Following initialization, the watchdog timer will time out after time T<sub>TO</sub> unless at least one  $\overline{\text{TCL}}$  pulse clears it. On timeout the reset pins reactivate for a further T<sub>TO</sub> period before deactivating again for another try. A  $\overline{\text{TCL}}$  pulse will deactivate any timeout reset, and another  $\overline{\text{TCL}}$  pulse must follow within a time T<sub>TO</sub> to keep reset inactive. If no  $\overline{\text{TCL}}$  pulses come at all, the reset pins go square-wave. Power-down overrides all this however. A falling voltage on V<sub>IN</sub> gives a warning  $\overline{\text{SAVE}} = 0$  signal at V<sub>IN</sub> = V<sub>SL</sub> before activating the reset pins as soon as V<sub>IN</sub> drops below V<sub>RL</sub>. The H6061 has fixed thresholds and low hysteresis for monitoring regulated DC lines. Additional protection is provided in case V<sub>DD</sub> supply falls over about 10% below V<sub>ON</sub> which thereupon activates all outputs at once.

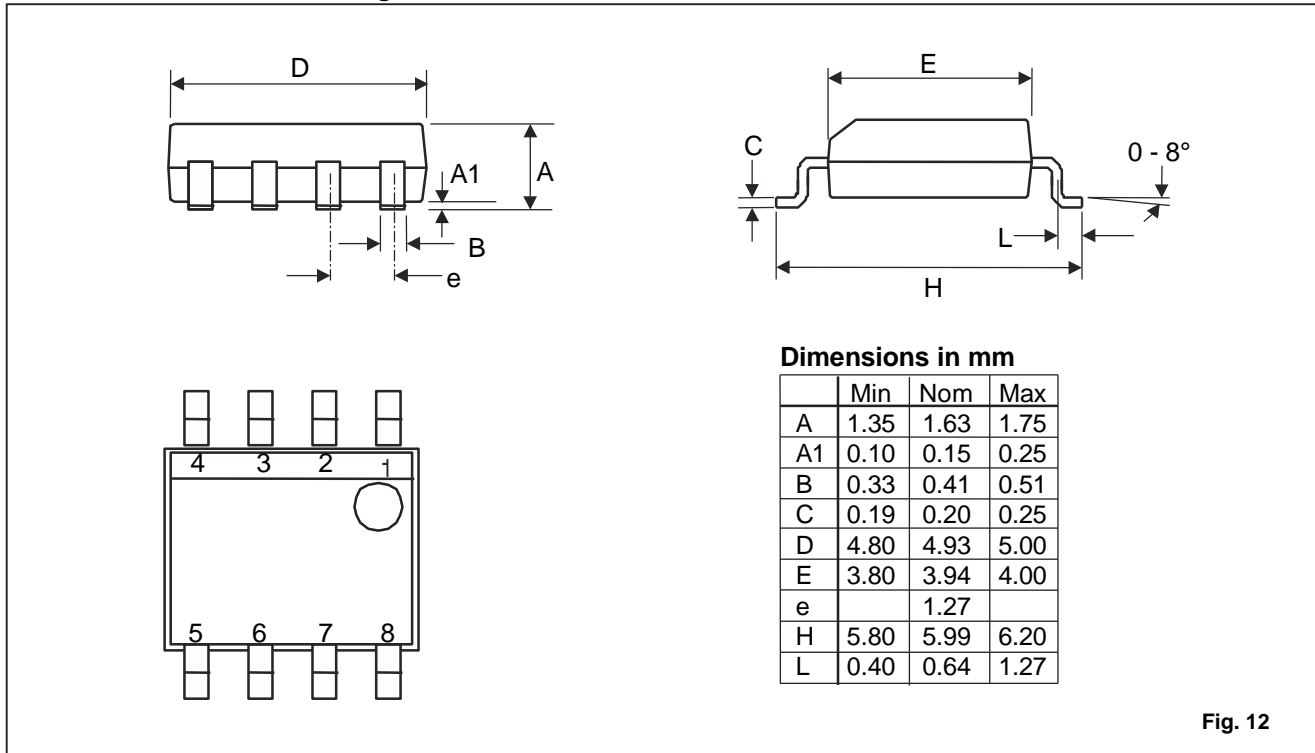


**Combined Supply Monitor, Initializer and Watchdog**



**External Programming of RC Oscillator**



**Package Information**  
**Dimensions of 8-Pin SOIC Package**

**Ordering Information**

When ordering, please specify the complete Part Number

Part Number	Version	Package	Delivery Form	Package Marking (first line)	Temperature
H6061V25SO8A	V25	8-pin SOIC	Stick	606125	-40°C to +85°C
H6061V25SO8B		8-pin SOIC	Tape&Reel	606125	

**Note:** other versions are no longer available

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